Inorganic Micro/Nanostructures-based High-performance Flexible Electronics for Electronic Skin Application

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Abstract

Electronics in the future will be printed on diverse substrates, benefiting several emerging applications such as electronic skin (e-skin) for robotics/prosthetics, flexible displays, flexible/conformable biosensors, large area electronics, and implantable devices. For such applications, electronics based on inorganic micro/nanostructures (IMNSs) from high mobility materials such as single crystal silicon and compound semiconductors in the form of ultrathin chips, membranes, nanoribbons (NRs), nanowires (NWs) etc., offer promising high-performance solutions compared to conventional organic materials. This thesis presents an investigation of the various forms of IMNSs for high-performance electronics. Active components (from Silicon) and sensor components (from indium tin oxide (ITO), vanadium pentaoxide (V_2O_5), and zinc oxide (ZnO)) were realised based on the IMNS for application in artificial tactile skin for prosthetics/robotics.

Inspired by human tactile sensing, a capacitive-piezoelectric tandem architecture was realised with indium tin oxide (ITO) on a flexible polymer sheet for achieving static (upto 0.25 kPa^{-1} sensitivity) and dynamic (2.28 kPa^{-1} sensitivity) tactile sensing. These passive tactile sensors were interfaced in extended gate mode with flexible high-performance metal oxide semiconductor field effect transistors (MOSFETs) fabricated through a scalable process. The developed process enabled wafer scale transfer of ultrathin chips (UTCs) of silicon with various devices (ultrathin chip resistive samples, metal oxide semiconductor (MOS) capacitors and n-channel MOSFETs) on flexible substrates up to 4″ diameter. The devices were capable of bending upto 1.437 mm radius of curvature and exhibited surface mobility above 330 cm^2/V-s, on-to-off current ratios above 4.32 decades, and a subthreshold slope above 0.98 V/decade, under various bending conditions.

While UTCs are useful for realizing high-density high-performance micro-electronics on small areas, high-performance electronics on large area flexible substrates along with low-cost fabrication techniques are also important for realizing e-skin. In this regard, two other IMNS forms are investigated in this thesis, namely, NWs and NRs. The controlled selective source/drain doping needed to obtain transistors from such structure remains a bottleneck during post transfer printing. An attractive solution to address this challenge based on junctionless FETs (JLFETs), is investigated in this thesis via technology computer-aided design (TCAD) simulation and practical fabrication. The TCAD optimization implies a current of 3.36 mA for a 15 μm channel length, 40 μm channel width with an on-to-off ratio of $4.02x\ 10^7$. Similar to the NRs, NWs are also suitable for realizing high performance e-skin. NWs of various sizes, distribution and length have been fabricated using various nano-patterning methods followed by metal assisted chemical etching (MACE). Synthesis of Si NWs of diameter as low as 10 nm and of aspect ratio more than 200:1 was achieved. Apart from Si NWs, V_2O_5 and ZnO NWs were also explored for sensor applications. Two approaches were investigated for printing NWs on flexible substrates namely (i) contact printing and (ii) large-area dielectrophoresis (DEP) assisted transfer printing. Both approaches were used to realize electronic layers with high NW density. The former approach resulted in 7 NWs/μm for bottom-up ZnO and 3 NWs/μm for top-down Si NWs while the latter approach resulted in 7 NWs/μm with simultaneous assembly on 30x30 electrode patterns in a 3 cm x 3 cm area. The contact-printing system was used to fabricate ZnO and Si NW-based ultraviolet (UV) photodetectors (PDs) with a Wheatstone bridge (WB) configuration. The assembled V_2O_5 NWs were used to realize temperature sensors with sensitivity of 0.03% /K. The sensor arrays are suitable for tactile e-skin application.

While the above focuses on realizing conventional sensing and addressing elements for e-skin, processing of a large amount of data from e-skin has remained a challenge, especially in the case of large area skin. A Neural NW Field Effect Transistors (υ-NWFETs) based hardware-implementable neural network (HNN) approach for tactile data processing in e-skin is presented in the final part of this thesis. The concept is evaluated by interfacing with a fabricated kirigami-inspired e-skin.

Apart from e-skin for prosthetics and robotics, the presented research will also be useful for obtaining high performance flexible circuits needed in many futuristic flexible electronics applications such as smart surgical tools, biosensors, implantable electronics/electroceuticals and flexible mobile phones.

Declaration

Unless otherwise acknowledged, the content of this Thesis is the result of my own work. None of this material has been submitted for any other degree at the University of Glasgow or any other institution.

William Ringal Taube Navaraj

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16. W. Taube Navaraj**,** O. Ozioko and R. Dahiya, *A Spiking Neural Network Classifier System interfaced to a Fingerprint-enhanced Biomimetic Tactile Sensor,* Invited as extended paper of IEEE-Sensor, In progress.
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Contributors

Some of the work presented mainly in chapter 7 of this thesis were done in collaboration with Carlos Garcia Nunez (C. G. N.), Dhayalan Shakthivel (D. S.) and Fengyuan Liu (F. L.).

The idea of temperature-assisted dip coating for large-area nanosphere lithography was conceptualised by me and the initial experiments for the assembly were carried out by me. I also contributed in deciding the motors, other specifications and configurations of the dip coater. Later, the optimisation was carried out and lead by C. G. N. with support from F. L. All four of us contributed to the work through regular discussions. C. G. N. and myself are equal contribution first authors in the resulting publication.

Regarding the contact printing of nanowires (NWs) and the resulting UV sensor array, C. G. N. and F. L. synthesised ZnO NWs. Hence, the synthesis of ZnO NWs is not presented in this thesis. Myself and D. S. synthesised the Si NWs. I contributed in the contact printing setup in terms of deciding the motors, load cell arrangement, and the configuration for printing. Whatever figures from publication where MACE-synthesised Si NWs are involved are included in this thesis for the sake of completion. C. G. N. played a lead role in building the contact printing setup, carried out the optimisation of the process with support from F. L. I further contributed through discussion/implementation of UV dosimeter for wearable application and the Wheatstone bridge array configuration.

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Contents

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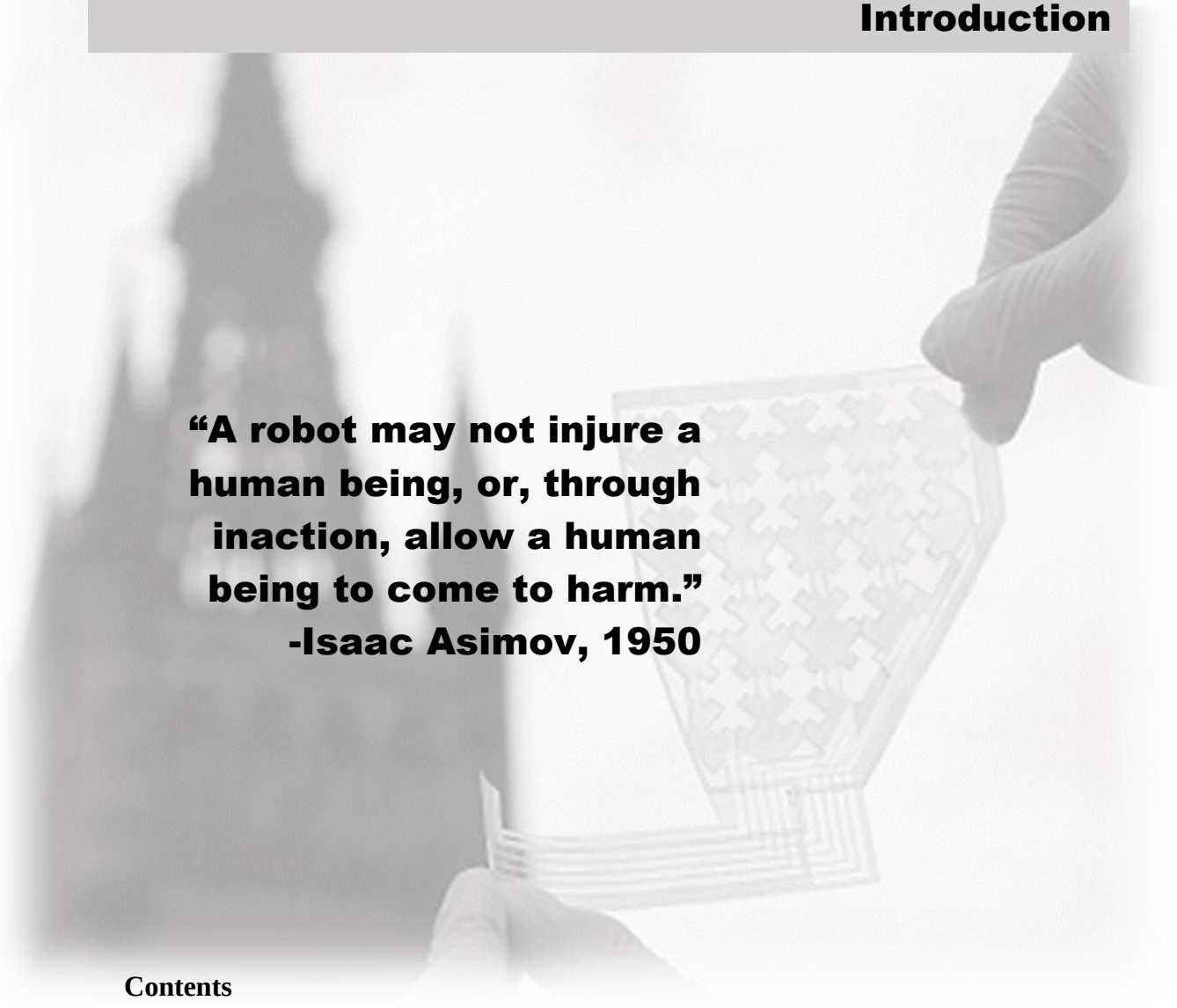
List of Acronyms

AFM	-	Atomic Force Microscope
ALD	-	Atomic Layer Deposition
APCVD	-	Atmospheric Pressure Chemical Vapour Deposition
BSS	-	Beam Step Size
CV	-	Capacitance Voltage
DEP	-	Dielectrophoresis
E-skin	-	Electronic Skin
EBL	-	Electron Beam Lithography
ECG	-	Electro-cardio-graphy
EMG	-	Electro-myo-graphy
FET	-	Field Effect Transistor
HMDS	-	Hexa Methyl Di-Silazane
IC	-	Integrated Circuit
ICP-CVD	-	Inductively Coupled Plasma Chemical Vapour Deposition
IoT	-	Internet-of-Things
IPA	-	Isopropyl Alcohol
JLFET	-	Junctionless Field Effect Transistor
LB	-	Langmuir Blodgett
LED	-	Light Emitting Diodes
LPCVD	-	Low Pressure Chemical Vapour Deposition
MACE	-	Metal Assisted Chemical Etching
MBE	-	Molecular Beam Epitaxy
MEMS	-	Micro Electro Mechanical Systems
MOCVD	-	Metal Organic Chemical Vapor Deposition
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NSL	-	Nano sphere lithography
NW	-	Nanowire
PDMS	-	Poly Di-Methyl Siloxane
PECVD	-	Plasma Enhanced Chemical Vapor Deposition
PI	-	Polyimide
PLD	-	Pulse Laser Deposition

POSFET	-	Piezoelectric Oxide Semiconductor Field Effect Transistor
PTFE	-	Poly Tetra Fluoro Ethylene
PVD	-	Physical Vapour Deposition
RF-ID	-	Radio Frequency Identification
RH	-	Relative Humidity
RT	-	Room Temperature
SEM	-	Scanning Electron Microscope
SMU	-	Source Measure Unit
SOI	-	Silicon on Insulator
SP	-	Micro/Nano-spheres
TFT	-	Thin Film Transistor
ULSI	-	Ultra-Large Scale Integration
UTC	-	Ultra-Thin Chips
UTS	-	Ultra-Thin Structures
UV	-	Ultra-Violet
VLS	-	Vapour-Liquid-Solid
VRU	-	Variable Resolution Unit
µLED	-	Micro Light Emitting Diode
ν-NWFET	-	Neural Nanowire Field Effect Transistor

1

Introduction



“A robot may not injure a human being, or, through inaction, allow a human being to come to harm.”
-Isaac Asimov, 1950

Contents

1. Introduction

1. 1. Motivation

Flexible electronics is considered to be one of the key next generation technologies currently pursued by researchers around the world. This field boasts a strongly emerging market[1]. Forecasts suggest that the market for printed flexible sensors alone will reach $300 billion by 2028 [2,3].

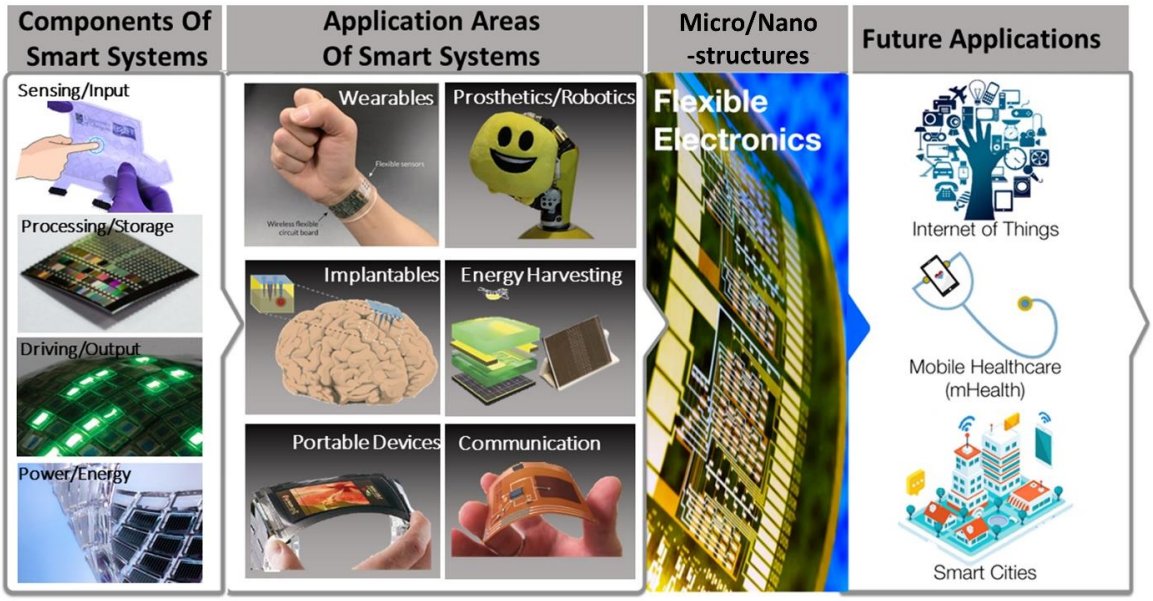


Fig. 1-1: Applications enabled by inorganic micro-/nanostructures based high-performance flexible electronics through underpinning research in areas such as sensing, computing, data storage and energy. Adapted from [4]. npj:CC by 4.0. References: [5-9].

Fig. 1-1 shows the various application areas of smart flexible electronic devices and systems which demonstrate that flexible electronics is revolutionizing the way we could use electronics in the future. The progress in this field is driven by application areas that require bendability, such as wearables, implantables, portable devices, energy harvesting and tactile e-skin for robotics/prosthetics. In turn, this progress is enabling the development of numerous futuristic applications, such as mHealth, smart cities, and Internet-of-Things (IoT). Such applications, for efficient realisation, require intense heterogeneous integration among some of the following components: various physical sensors (such as tactile, pressure, strain, acoustic, magnetic, thermal, optical) and chemical sensors, flexible display devices (light emitting diodes(LED)), thin film transistors (TFTs), energy harvesting devices (such as photovoltaics, thermo-electrics, tribo-electrics), interconnects, antennas etc.[1]

Currently, organic materials are widely used for flexible electronic devices due to their inherent mechanical flexibility and relatively low material and processing costs. However, organic materials typically have low charge-carrier mobility (0.0001-10 $cm^2/V.s$ in contrast to 100-3000 $cm^2/V.s$ of inorganic semiconductors) [10-13], which makes them unsuitable for high-performance flexible electronics. A range of alternative solutions is therefore being explored for high-performance flexible electronics. For example, two-dimensional (2D) materials such as graphene, which have very high charge-carrier mobility, are being explored as channel materials for Field Effect Transistors (FET) [14]. However, graphene's zero bandgap and difficulties with its synthesis and transfer over large flexible areas pose a huge

challenge [14]. Although there is some progress in this direction, the technology is still not at a stage where one can think of large-scale integration.

Several current and future flexible electronics (Fig. 1-1) would require fast communication and computation. For example, faster memories and large drive currents are necessary in applications such as flexible portable display devices. Likewise, wireless communication in mHealth or IoT will require switching in frequency bands up to ultra-high frequencies (0.3 – 3 GHz)[15]. The faster communication, higher bandwidth, and efficient distributed computation implemented with the very high switching speeds required for IoT or smart cities, will make the high-performance requirements inevitable to achieve smart connected objects with flexible nodes.

In this regard, micro/nanostructures, such as ultra-thin chips, thin membranes, ribbons, nanowires etc. from single crystal silicon and compound semiconductors can offer better solutions as they exhibit high charge-carrier mobility and the technology for devices based on these materials is mature [16,13,17]. Fig. 1-2 gives a schematic illustration of multiple forms of Si and other inorganic micro/nanostructures (IMNSs) for high-performance flexible electronics. Bulk silicon is normally rigid and brittle; but, in thin form factors it starts to become flexible (e.g. ultra-thin silicon wafer (Fig. 1-2b) or chips (Fig. 1-2c)). Thin silicon was initially explored as a means to realize photovoltaic arrays for space applications[18]. The technology readiness available to obtain devices down to nanoscale dimensions and the possibility to exponentially scale the device densities with Ultra-Large Scale Integration (ULSI) up to billions of devices per cm^2, makes silicon-based microelectronics a good candidate for addressing immediate high-performance needs in flexible electronics in the form of ultra-thin chips [4]. Furthermore, recent advances, such as the printing of silicon and compound semiconductor micro/nanostructures on flexible substrates make them an attractive alternative for high-performance large-area flexible electronics [19-22]. To realize electronics by printing, silicon-based membranes/ribbons and wires as active components (e.g. FETs) are among the best potential candidates (FETs structures schematically illustrated in Fig. 1-2(d and e). Other approaches such as thick chip array on foil (Fig. 1-2f) and polycrystalline inorganic materials, (Fig. 1-2g) such as poly-silicon or metal oxides [1] on flexible substrates are also potential candidates depending on the application of interest. The above implies that inorganic micro/nanostructure (IMNS) based bendable high-performance electronics could lead to a wide range of applications. This thesis focuses on synthesis, transfer printing of inorganic material nanostructures and development of high-performance flexible electronics. The primary application targeted and investigated in this thesis is realizing e-skin for next generation prosthesis and robotics.

A 2013 survey of amputees indicated that the two most critical elements for a wide-spread acceptance of prosthetics are (1) the ability to feel with their prostheses and (2) enhanced, intuitive motor control[23]. Without sensory feedback, the prosthetics will be just like any other tool and won't become a 'part of the body' of the amputee for intuitive use. Research shows that subjects tend to apply much more force than necessary when carrying out tasks involving their fingers and hands when the hands are temporarily anaesthetised [24]. Research also suggests that those who lose their sense of touch constantly suffer bruises, burns and broken bones due to the lack of sensory feedback [24]. The above indicates that the sense of touch plays an important role in understanding and interacting with various objects and environments and in carrying out the associated motor behaviours.

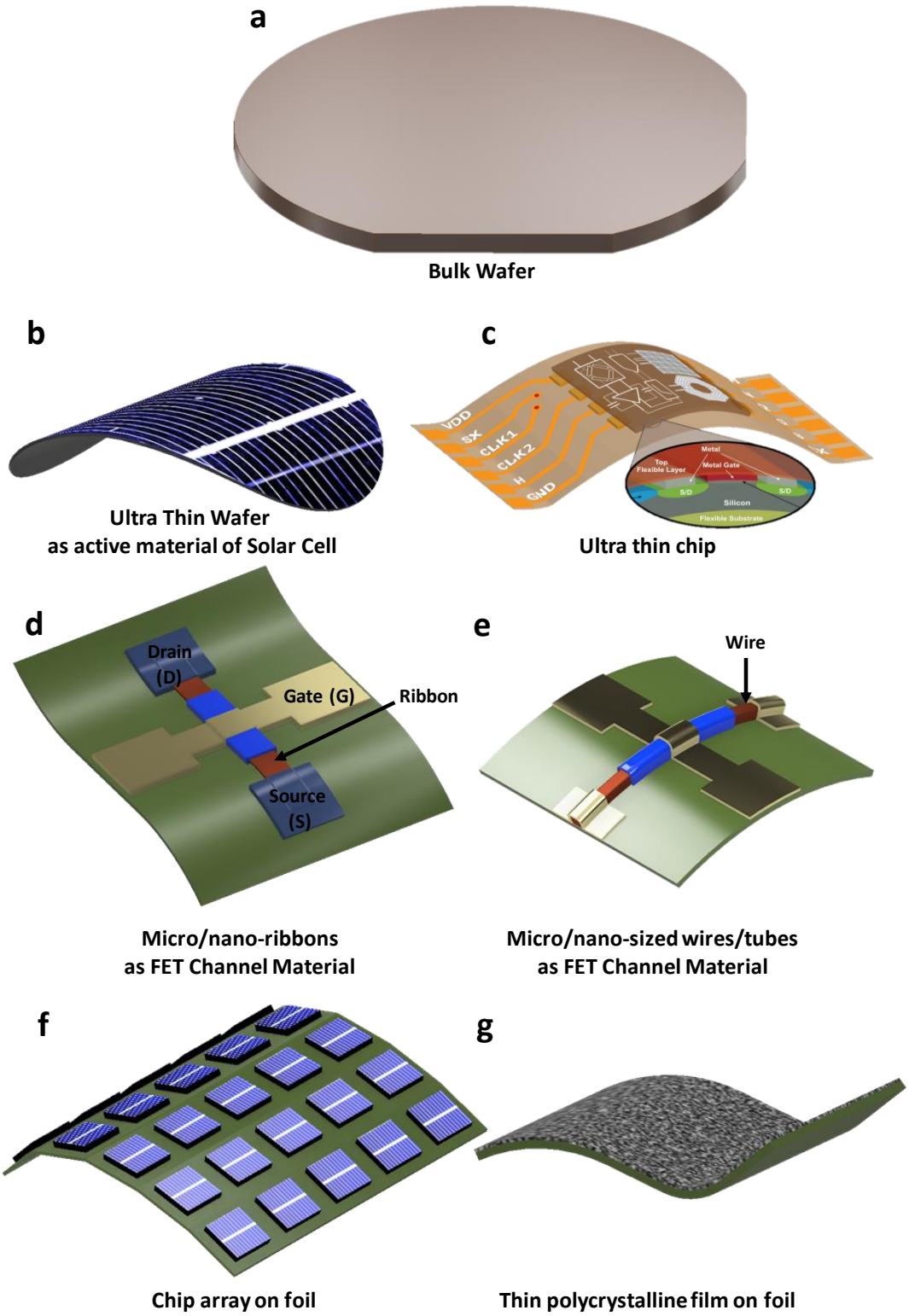


Fig. 1-2: Illustration of (a) bulk silicon and (b-g) multiple forms of inorganic semiconductors for flexible electronics.

Another important field is robotics, whereby rapid technological advancements are pointing to a future where robots will no longer be merely industrial tools but will be expected to work side by side with humans and assist them in their daily lives. Robotic technology will be useful in applications such as robotic-assisted surgery, exoskeletons, social robots, education, assistive chefs etc. However, achieving safe interaction between robots and humans and effectively dealing with environmental uncertainties is an important challenge to be solved before robots can be used for day-to-day applications. While visual

and auditory sensing are being widely studied by robotic researchers, a sense of touch is important for the robots to achieve safe interaction with humans and operate in their associated highly complex and dynamic world. Compared to visual and auditory sensing, tactile sensing has yet to receive as much attention by robotic researchers despite its importance. The primary reason for this is the complexity associated with developing such a system requiring a significant number of sensors distributed over a large area compared to other sensing modalities which are more localised. In addition, the tactile sensing system requires flexibility and conformability to the various shapes of robots [22]. Flexible high-performance components which can be fabricated over a large area cost effectively is critical to achieving this. IMNSs are ideal candidates for realizing high-performance components for electronic skin. The second chapter summarises the specifications for e-skin and discusses how IMNSs can be used to achieve high-performance flexible electronics for realizing such applications.

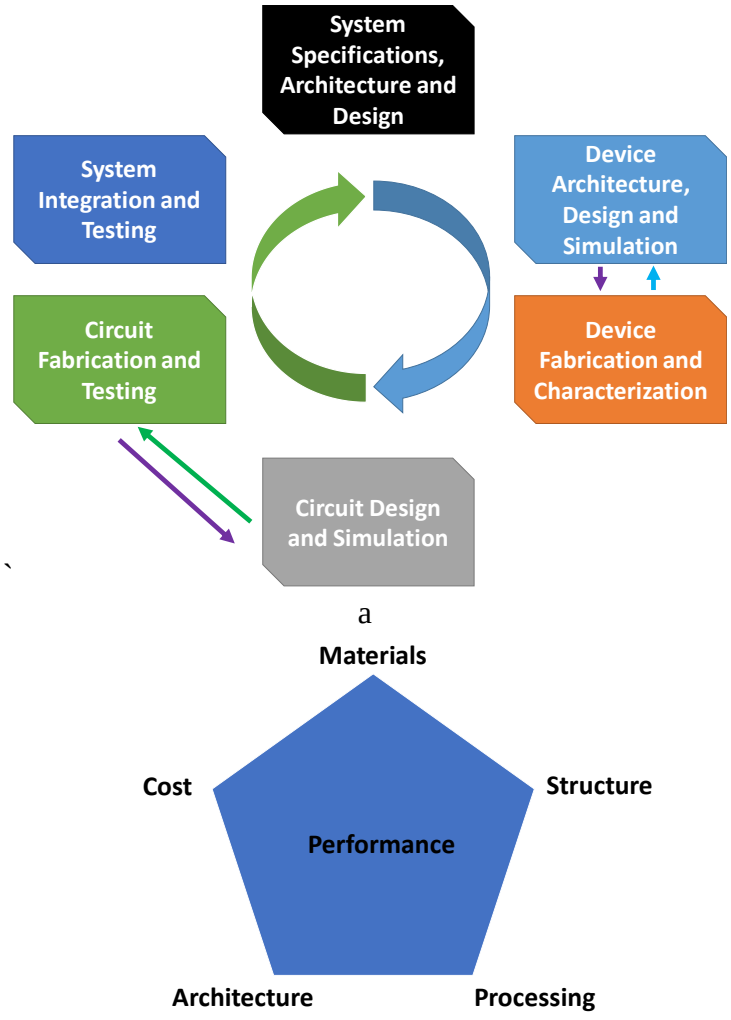


Fig. 1-3: (a) Flexible Electronics System Development Cycle (b) Components to be considered for flexible electronics system

The two important aspects to be considered for realizing most common electronic systems are shown in Fig. 1-3 (a and b), namely the system development cycle and the key components; the same applies for the development of a flexible electronic skin system. The cycle starts with system specifications followed by the design of the system architecture. Computing requirements, energy/power requirements, various modules, speed, form factor,

design, and compatibility are all typical aspects that should be taken into consideration for the system design. Some of these are discussed with reference to an electronic skin system in chapter 2 of this thesis. Then, various device architectures must be decided, considering the system specifications and the performance needed. The various components given in Fig. 1-3b play an important role in deciding the device performance, namely, the materials, microstructure, processing, architecture and cost. All of these components are interrelated. For example, the architecture and material used detemine the processing requirements which, in turn, affect the microstructure of the material which eventually affects the associated cost. Advanced flexible electronic system development requires modelling/simulation studies on various levels, namely, on a device, circuit and system level. The device level work flow (involving simulation, fabrication and characterisation) may require iterations before finalizing a device component. Empirical parameters, such as fixed oxide charges, interface trap density of gate dielectric and mobility of channel material, are required to be fed as input to MOSFET models in order to obtain accurate device simulation characteristics. The overall flow goes through cycles of device, circuit and system for further advancements and price-performance enhancement. The major focus of this thesis is on developing various sensor and device components to achieve a tactile sensing system based on IMNSs while attempts have been made to realize this upto system level implementation. In this thesis, all the individual components of Fig. 1-3a and b have been dealt with.

1. 2. Objectives, Original Contributions and Key Advancements

This research has two main objectives:

1) To develop technologies for realizing high-performance electronics by using inorganic micro/nanostructured materials (primarily silicon). Figure of merits of high-performance include mobility, on-to-off ratio, subthreshold slope, bending stability, switching and transit frequency.
2) To apply the above technology as a means to realize an electronic skin system for prosthesis/robotics.

The following are my original contributions established during this PhD research for achieving the above objectives and the associated key advancements to the state-of-the-art:

1) **Tactile Sensors:** Fabricated capacitive-piezoelectric tandem architecture sensor for biomimetic tactile sensing from indium tin oxide (ITO) thin film on poly ethylene terephthalate (PET) sheet. The capacitance-piezoelectric tandem architecture for biomimetic tactile sensing was investigated for the first time. Further, the architecture of the capacitive component with projected floating electrode is a novel structure which is studied for the first time. This leads to capacitive tactile sensor which are independent of the material making the contact compared to conventional capacitive touch screen which will respond only to conductive material. Further the structure leads to a nonlinear sensitivity similar to human tactile sensing with very high sensitivity (up to 0.25 kPa^{-1}) in the lower pressure (<100 Pa) range while lower sensitivity in higher pressure (0.002 kPa^{-1} at ~2.5 kPa). This tandem structure helps for both quasi-static and dynamic tactile exploration for example both static and dynamic feedback can be provided to the prosthesis users as explained in the final section of this thesis. Further, for tactile exploration application, the static sensor serves to maintain a stable pressure while the dynamic sensor can provide the details of texture variation which are suitable for accurately distinguishing or classifying tactile samples.

2) **Ultra-thin Silicon Wafer/Chip:** Carried out synthesis and wafer scale transfer of ultra-thin silicon chips with devices such as silicon MOS capacitors and MOSFETs. The MOSFETs were used in an extended gate configuration with the capacitive-piezoelectric tandem architecture tactile sensor modules. The various processes and results are presented in chapter 5 and are also partly published in a journal publication [25]. As highlighted in the publication, this is for the first-time wet etching has been used to realize ultra thin chips from bulk silicon upto 4 inch scale. The transfer printing process demonstrated upto 4-inch scale also advances the state-of-the-art (few cm scale prior work). The mobility of >330 $cm^2/V.s$ is several times higher compared to that of organic materials-based transistor (0.0001-10 $cm^2/V.s$) conventionally used for flexible electronics.
3) **Ultra-thin Silicon Membrane/Ribbon:** Conceptualised and simulated ultra-thin silicon ribbon based junctionless FETs (JLFET) for use in high-performance flexible printable electronics. This addresses the challenges associated with selective source/drain doping and realizing printable CMOS circuits with inorganic nanostructures. Metal with optimised work function is used as a gate electrode to enable low temperature deposition in contrast to conventional JLFETs using polysilicon of opposite polarity for gate formation with normally-off operation. By tuning the work function of the metal gate, normally-off operation can be achieved. The results of the simulations are published in [26].
4) Optimised transfer printing of ultra-thin silicon ribbons and fabricated ribbon based JLFETs. The concept and results are discussed in chapter 6. This is the first-time JLFET technology is explored for high-performance flexible electronics.
5) **Nanowires:** Conceptualised and was involved in the development of large-area self-assembly of silica microspheres/nanospheres (also known as nano-sphere lithography (NSL)) by temperature-assisted dip-coating. The assembled spheres were used to synthesize silicon nanowires by metal assisted chemical etching (MACE), a top down fabrication process. The concept and results are discussed in chapter 7 and are part of the publications [27,28]. The synthesised wires were heterogeneously integrated with bottom-up fabricated ZnO nanowires to realize ultra-violet (UV) dosimeter arrays which has resulted in publications [29-31]. Approaches such as Langmuir-Blodgett and charge reversible substrates requires the surface functionalization of SPs (or substrate). The key advancement of the work reported here, with respect to conventional dip-coating procedures, include the larger micro/nanospheres self-assembled monolayers (SAMs) surface coverages and better control over the SPs SAM stripe-pattern morphology by using temperature-assisted dip-coating approach. The area over which SAMs are formed can be controlled by tuning the suspension temperature (T_s), which allows precise control over meniscus shape. Furthermore, the formation of periodic stripes of SAM, with excellent dimensional control (stripe width and stripe-to-stripe spacing), is demonstrated using a suitable set of dip-coating parameters. The optimization allowed the SAM formation over areas (2.25 cm^2) roughly 10 times larger than reported in literature using nanospheres.
6) Synthesised silicon nanowires using a modified nanosphere lithography and e-beam dots-on-the-fly process followed by MACE. The work has resulted in a conference presentation [28]. Conceptualised and was involved in the development of large area dielectrophoresis (DEP) for templated transfer printing of nanowires for developing circuits from it. The contactless large-area DEP resulted in 7 NWs/μm simultaneous

assembly on 30x30 electrode patterns in a 3 cm x 3 cm area. The process is scalable to far bigger areas and the template is reusable compared to conventional DEP.

7) Conceptualised and simulated in device, circuit and system level ν-NWFET as a building block towards a biomimickry electronic skin. Fabricated sample ν-NWFET and characterised it. The work has resulted in publications and conference presentations [32,33]. The viability of Si nanowires (NWs) as the active material for υ-NWFETs in HNN is explored through modelling and demonstrated by fabricating the first device. Using υ-NWFETs to realize HNNs is an interesting approach as by printing NWs on large area flexible substrates it will be possible to develop a bendable tactile skin with distributed neural elements (for local data processing, as in biological skin) in the backplane.
8) **Prosthesis Interface:** Involved in the development of self-powered 3D printed bionic hand with a kirigami-inspired electronic skin. Some of the publications related to skin interface with prosthesis are [34,35] . The key advancements in the developed prosthesis are: biomimetic tactile sensing, a kirigami-inspired patterning strategy to conformally cover the prosthesis, surface myoelectric-controlled with capability to static and dynamic force feedback[36,37], flexible solar-cell array and supercapacitors for energy harvesting. The last component was done in collaboration with others[38].

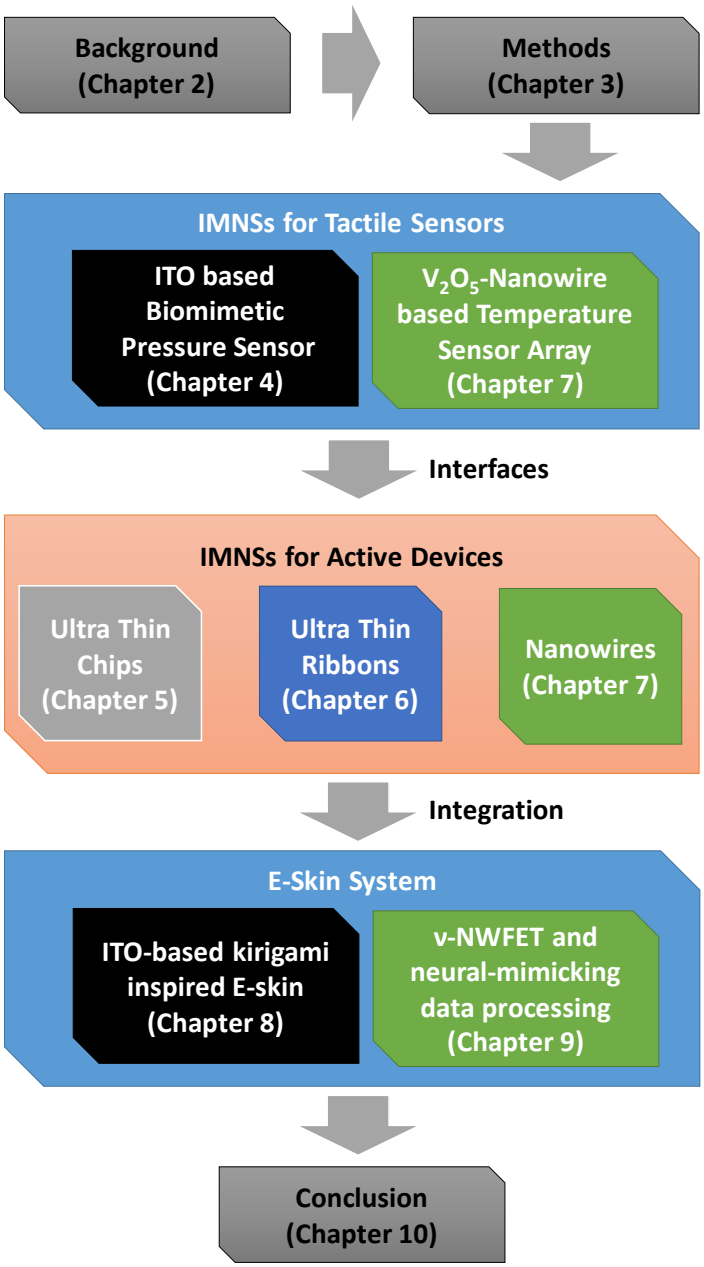


Fig. 1-4: Organisation of thesis

1. 3. Organisation of Thesis

The rest of the report is organised as shown in Fig. 1-4 and outlined below:

Chapter 2 presents a background and review of relevant literature. Initially, there is a discussion on material aspects and why IMNS is useful for high-performance flexible electronics. This is followed by a discussion on the multiple forms in which IMNSs could be used, namely in the form of ultra-thin silicon chips, ultra-thin membranes, microwires, and nanowires. The properties of IMNSs, strategies for fabrication/synthesis, transfer printing and realisation of devices/circuits for flexible electronics are also presented. A section is dedicated here on how bending and stress affect the electrical properties of silicon of various form factors. Specifications for an advanced electronic skin (e-skin) system and for how IMNSs can find a role for realizing e-skin both for the perspective of robotics as well as prosthesis are provided.

Chapter 3 presents details on the various simulation/modelling and experimental tools employed to carry out the outlined research work. The simulation/modelling tools include Silvaco TCAD, Matlab, Multisim and SimBrain. The experimental tools include electron beam evaporation, thermal evaporation, plasma-enhanced chemical vapour deposition (PECVD), semiconductor parameter analyser, photolithography, electron beam lithography, dielectrophoresis setup, and optical and electron microscopes.

Chapter 4 presents capacitive-piezoelectric tandem architecture passive sensors for biomimetic tactile sensing in a prosthetic hand.

Chapter 5 discusses ultra-thin chips (UTCs) of Si for application in high-performance flexible electronics. Fabrication, transfer printing and the results from fabricated UTC are presented in this chapter. The results of active extended gate tactile sensors by interfacing sensor structures depicted in chapter 4 with the fabricated MOSFETs are presented here.

Chapter 6 explores how nanoribbons are useful for high-performance flexible electronics. Synthesis, transfer printing and the results from fabricated UTCs are presented in this chapter. The concept and simulation results of ultra-thin silicon-ribbon-based JLFETs for use in high-performance flexible printable electronics are discussed. Optimisation of transfer printing of ultra-thin silicon ribbons and fabrication of JLFETs are presented.

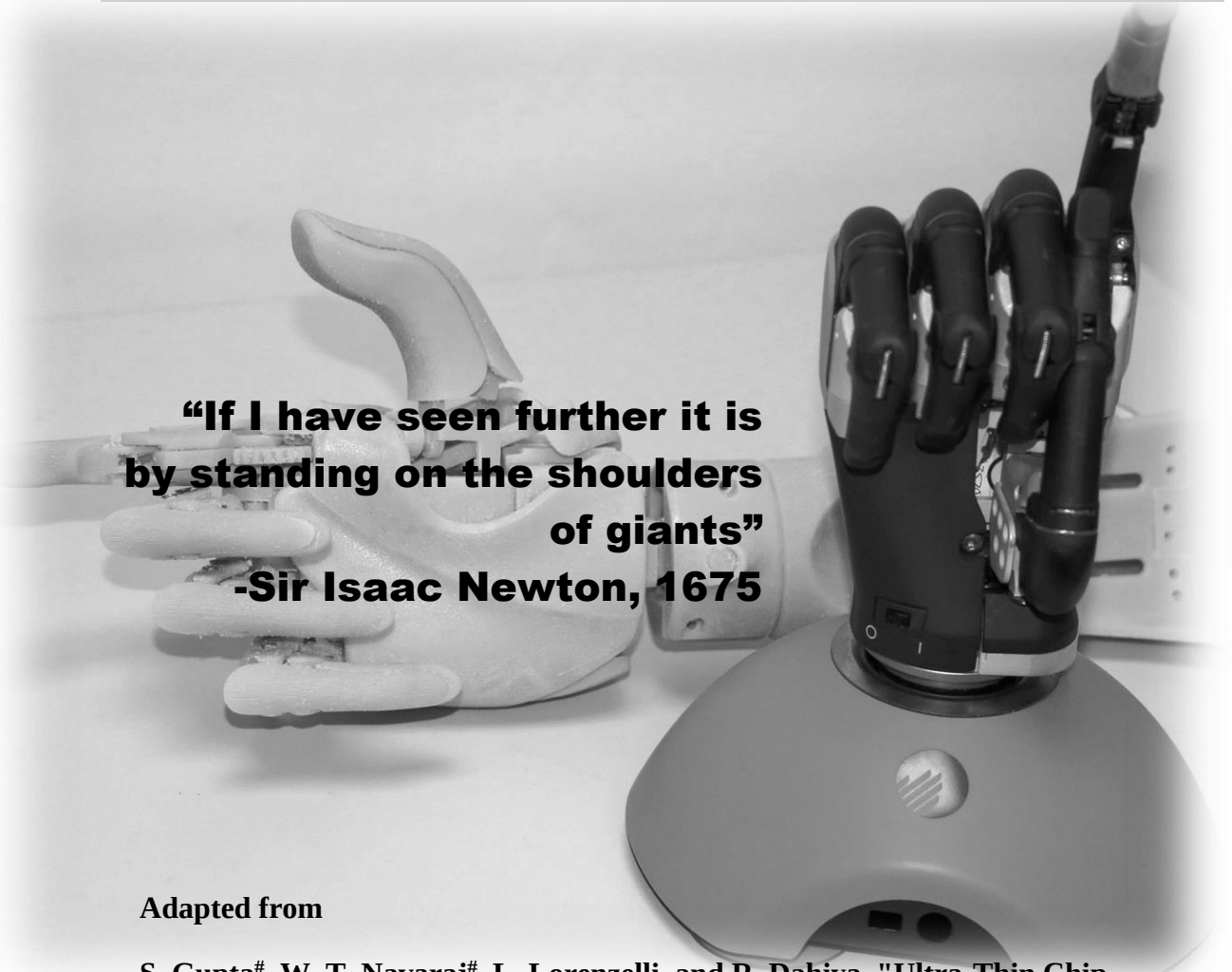
Chapter 7 is dedicated to the synthesis and transfer printing of nanowires. Work related to large-area self-assembly of silica microspheres/nanospheres by temperature-assisted dip-coating is presented. Silicon nanowires were synthesised using nanosphere lithography, modified nanosphere lithography and dots-on-the-fly electron beam lithography followed by MACE. Contact printing and large-area dielectrophoresis assisted printing of nanowires are documented in this chapter. The results from various strategies will be analysed and compared so as to achieve high-performance in flexible electronics. The overall aim will be to realize single crystalline, non-porous nanowires with appropriate dimensions, areal densities and electronic properties, such as mobility. The influence of experimental conditions, such as etchant concentration, etch duration and catalyst metal will be discussed in detail. The developed templated contactless dielectrophoresis (DEP) process for aligned large area nanowire transfer printing will also be discussed in this chapter.

Chapter 8 is dedicated to e-skin. E-skin requires an integration of sensors and electronics. Here, flexible indium tin oxide (ITO) thin film on PET sheet has been used to make individual sensory elements and arrays. To make the skin conformably cover a bionic hand, inspiration from Kirigami was used in the design and fabrication which was eventually integrated to a bionic hand. This skin was interfaced to a nanowire based neuromimicking processing system. The results of simulation in device, circuit and system level of ν-NWFET electronics as a building block towards a biomimicking e-skin and results from the fabricated sample ν-NWFET are presented.

Chapter 9 puts forth the conclusion section summarizing the thesis and is followed by a discussion of open problems for future development.

2

Review of Literature



“If I have seen further it is by standing on the shoulders of giants”
-Sir Isaac Newton, 1675

Adapted from

S. Gupta[#], W. T. Navaraj[#], L. Lorenzelli, and R. Dahiya, "Ultra-Thin Chip Technologies for High-performance Flexible Electronics", NPJ Flexible Electronics, 2018, [#]Equal Contribution, [4] npj:CC by 4.0.

Contents

2. Review of Literature

2. 1. Need of IMNSs for High-Performance Flexible Electronics

Electronic devices and integrated circuits are conventionally fabricated on rigid and flat substrates such as silicon (Si) wafers as current micro/nanofabrication technology allows realizing devices on planar substrates only. Resulting planar electronics has revolutionised our lives through fast communication and computing, but the lack of bendability in these devices presents challenges for using them in emerging applications such as wearable and implantable electronics, and robotic skin. These applications require high-performance electronics to conform to curved surfaces[39,40,16,41-46,34,47]. For this reason, there is a huge interest in obtaining electronics on flexible and non-conventional substrates such as soft plastics and even paper[48,1]. Fig. 1-1 in the previous chapter showed the various application areas of smart flexible electronic devices and systems. Flexible electronics is changing the way we make and use electronics. For example, the convergence of flexible electronics and biology has immense potential for many exciting future applications, some of these are implants, actuators, tools for surgical procedures, electrodes, sensors and neural interfaces. The key enablers for realizing such exciting applications are electronics that can be integrated intimately and conformally to the soft, curvilinear surfaces of biological tissues. Many existing applications such as wearable/implantable systems that require bendability to conform to the curved surface of tissues and organs[49] are driving the progress in the field, which in turn enable the development of numerous futuristic applications, such as mHealth, wearable systems, smart cities, and Internet-of-Things (IoT). Smartphones with roll-up displays and healthcare patches attached to the skin to deliver drugs or monitor vital signs etc. are some other areas which will benefit from electronics on flexible substrates[16,1,50]. Several initiatives from governments and industry have contributed to the progress in this important futuristic area and it is now estimated that the market for flexible electronics will reach $300 billion by 2028[51,52,2]. The high-performance, on par with today's Complementary Metal Oxide Semiconductor (CMOS) electronics, will be critical to this growth in flexible electronics as several current and future electronics would require fast communication and computation. For example, large drive currents and fast readout are needed in applications such as interactive flexible displays and flexible memory. Likewise, wireless communication in mHealth or IoT (where wearable sensor patches are needed for continuous measurements) will require data handling with communication in frequency bands up to ultra-high frequencies ($0.3 - 3\ GHz$)[15,53]. The faster communication, higher bandwidth, and efficient distributed computation with very high clock speeds will make the high-performance requirement inevitable in connected devices. This high-performance requirement calls for investigations into new materials, fabrication technologies, methodologies, and design techniques[54] – all of which influence the device performance. The bendability along with high-performance (e.g. fast transistor switching for faster computations and communication) is critical in these emerging applications.

Tremendous progress in the field of flexible electronics during the last decade has mainly come through organic semiconductors, thanks to their inherent flexibility. Organic semiconductor and amorphous Si are useful for large area electronics as they can be printed or coated over large areas to form active electronics such as display elements and thin film transistors resulting in low fabrication costs[55,51,56,57,19,58]. However, the modest performance that has thus far been possible with organic devices limits their utility to low-end applications such as passive RFID tags and OLED displays[48]. This is because of their

low mobility (~1 $cm^2/V.s$, maximum reported ~43 $cm^2/V.s$[59]) and the technological limitations present such as poor resolution of printers (currently best resolution is ~20 µm[19]). While applications such as flexible displays do not require high frequency operation, applications where data processing and communication are involved require high-performances (e.g. large drive currents, faster transistor switching etc.).

Table 1: Comparison between mobility, channel length and normalised cut-off frequency and on-to-off ratio of transistors fabricated using different materials[4]

Material	Mobility [cm^2/V-s]	Channel length reported [nm]	Transit Frequency [GHz]	I_{on}/I_{off}	References
Mono-crystalline Si	300-1200	14	4250	10^9	[60-62]
Amorphous Si	5-32	12500	1.15 x 10^{-3}	10^5	[63,64]
III-V semiconductors	400-12000	75	165	10^4	[65-68]
MoS_2	700	300	42	10^8	[69-72]
WS_2	234	6000	3.8	10^8	[73,74]
Pentacene	1.5	2000	11.4 x 10^{-3}	10^2	[75-77]
CVD Graphene	24,000	40	100	10^2	[78-81]

The transistor switching frequency is influenced by the mobility and channel length – while mobility is a material property, the channel length depends on the technology used. To demonstrate how various materials, relate to performance, Table 1 compares some of the materials used in flexible electronics. This comparison is in terms of carrier mobility (μ), channel length (L), transit frequency (f_t) and the I_{on}/I_{off} ratio of transistors that use these semiconducting materials as current channels. The transit frequency is a measure of the intrinsic speed of a transistor and is defined as the frequency at which the small-signal current gain of the device drops to unity while the source and drain terminals are held at ac ground. Neglecting the effect of source/drain junction capacitance, the transit frequency is given by [82]:

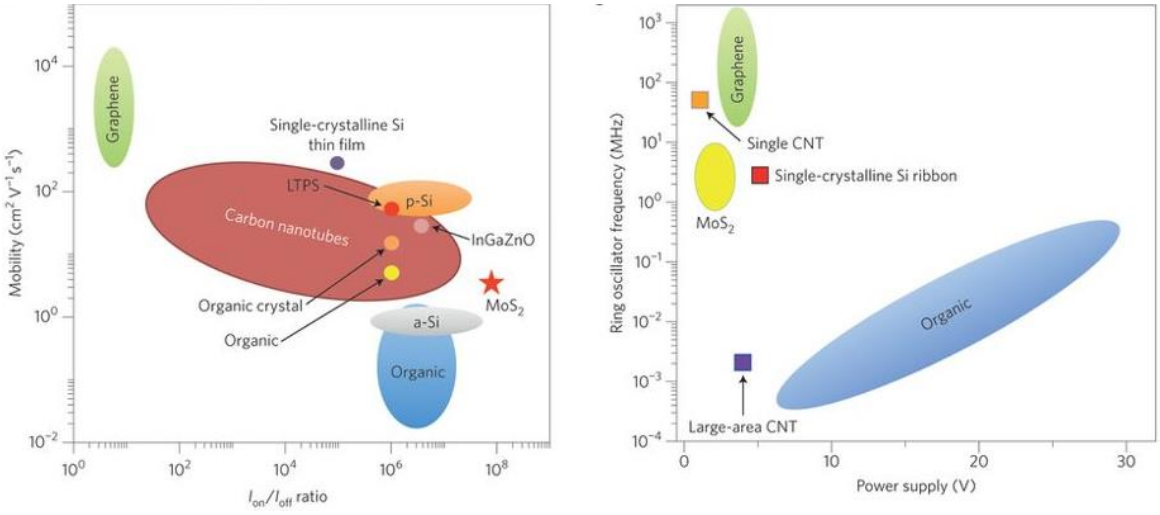
$$f_T = \frac{g_m}{2\pi(C_{GD}+C_{GS})} \quad \textbf{(E 2-1)}$$

Assuming fixed FET parameters such as channel width, oxide capacitance, gate-source capacitance etc. and fixed voltages such as terminal and threshold voltage, the dependency of transit frequency (which is a measure of transistor speed) boils down to mobility and channel length which can be expressed as [82]:

$$f_T = k\frac{\mu}{L^2} \quad \textbf{(E 2-2)}$$

where k is a proportionality constant arising from above stated assumptions. Normalizing Equation (1) with respect to the proportionality constant, the normalised transit frequency can be written as:

$$f_{T_{norm}} = \frac{f_T}{k} = \frac{\mu}{L^2} \quad \textbf{(E 2-3)}$$



(a) (b)

Fig. 2-1: Figures of merit of transistors with various materials typically used for flexible electronics (a) Trade-off between μ and I_{on}/I_{off} ratio (b) Operating frequency and voltage of ring oscillators. [83] Reprinted with permission from Springer Nature: Nature Nanotechnology vol. 9, 2014, Copyright 2014.

Thus, the f_{Tnorm} is directly proportional to the mobility and inversely proportional to the square of channel length when all the other parameters of the devices are considered the same. Based on the μ and L values from some of the recent works substituted in Eq. **2-2**, a comparison is given in Table 1. It shows that the monocrystalline silicon-based devices with channel length in the nanoscale regime will have high f_{Tnorm} and as a result will outperform most of the other semiconductor materials. Interestingly, the devices from high mobility materials such as graphene, carbon nanotubes[84] and some of the 2D materials are slower than silicon. Clearly, the channel length or device technology plays a significant role in the final performance of devices. Therefore, instead of solely fixating on high-mobility materials, a holistic view with inputs from both material science and engineering is important. Comparing these parameters, it is clear that the devices based on mono-crystalline Si and other inorganic semiconductor materials outperform organic materials. Although graphene, carbon nanotubes and some 2D materials have been reported to show higher mobility than Si, they are still in a nascent stage of process development and far from commercialisation[14,85]. The higher charge carrier mobility and shorter channel lengths enhance the speed of transistors[82]. On the basis of mobility (~1000 $cm^2/V.s$ for Si cf. ~1 $cm^2/V.s$ for organic semiconductors) alone, a Si based transistor will be 3 orders of magnitude faster than organic semiconductor or a-Si:H based devices[86,87]. Further, up to 9 orders of magnitude higher switching performance is achievable if small channel length (<100 nm with micro/nanofabrication cf. >20 μm with printing technologies) of Si devices is considered. Another important figure-of-merit to consider for high-performance electronics is the on-to-off (I_{on}/I_{off}) ratio of drain current of the transistor. High-performance transistors should have higher ON (drive) current and lower OFF (leakage) current. This is shown for different material systems schematically in Fig. 2-1a and tabulated for typical materials in Table 1. The bandgap of a material plays a critical role in deciding the I_{on}/I_{off} ratio, mainly the denominator (i.e.) the leakage or off current. With graphene being a zero-bandgap material, it has a very low I_{on}/I_{off} ratio despite being a high mobility material. Some organic materials have a high I_{on}/I_{off} ratio mainly because of their better sub-threshold performance, however, their lower mobility results in lower drive current. The best of both factors can be obtained by using silicon for realizing high-performance flexible electronics.

Considering these facts, the monocrystalline silicon, thanks also to its abundance, appears to be the best candidate to meet immediate high-performance needs of flexible electronic systems. This also explains why silicon and other materials such as compound semiconductors have attracted significant interest in recent years for flexible electronics. For this reason, new processing routes for the fabrication of high-performance flexible electronics with Si and other inorganic semiconductors have been recently explored[17,13] and constitute one of the prime goals of this thesis.

This chapter is organised into three further sections. Section 2. 2. presents multiple forms of IMNSs for high-performance flexible electronics. The same section describes the theoretical background where mechanical, electrical, optical and thermal properties are discussed of the various IMNSs. Section 2. 3. focuses on fabrication/synthesis of IMNSs and associated devices. The last section 2. 4. focuses on the application of IMNSs for tactile e-skin. Since the presented research focuses on tactile sensing, detailed account of IMNSs on tactile sensing has been presented in the last sub-section of this chapter.

2. 2. Multiple Forms of IMNSs for High-performance Flexible Electronics

Bulk silicon wafer (typical 2-12'' diameter, 150-500 µm thickness) in its fundamental form lacks flexibility and conformability which often puts hurdles in its effective utilisation in flexible and conformable electronics. The Si wafers start to lose their rigidity when they are thinned down to around 150 μm [88]. Between 50 and 100 μm, a wafer may fracture under its own weight. Below 50 μm the wafers get more flexible and more stable. Below 10 μm, a Si membrane is not only flexible but also starts to becomes optically transparent in certain regions of wavelength [47]. Thanks to the flexibility achievable through size reduction, silicon and other inorganic semiconductors could be used in various form factors such as: ultra-thin wafers, ultra-thin-chips, micro/nano-sized ribbons and micro/nanowires[89,12,46] for high-performance flexible electronics as schematically illustrated in Fig. 1-2. Ultra-thin-chips are mainly useful for high density, high-performance flexible micro/nanoelectronics circuits. Examples includes neural interface chips with massive array readout. Micro/nanosized ribbons and wires are suitable for large-area electronics also known as macroelectronics, achievable through large-scale synthesis of these structures and then using printing for fabricating the electronics. Examples include displays, electronic skin, active antennas, etc[13,90]. Furthermore, for achieving macro-level bendability, assembling islands of chips on a flexible substrate is one of the possible strategies as illustrated in Fig. 1-2f. Also, a polycrystalline thin film of inorganic materials on flexible foil/substrate can also be used for realizing high-performance electronics (Fig. 1-2g). In this thesis, investigation of the various forms of IMNSs for high-performance flexible electronics has been carried out. Primarily, they were used for realizing MOSFETs, passive and active tactile sensors and sensor arrays. While different IMNSs can be used for realizing high-performance flexible electronics the focus is given here mainly to silicon in various forms as the active material for MOSFETs. Other, inorganic materials such as Indium Tin Oxide (ITO) thin film on flexible PET substrate and Vanadium Pentoxide (V_2O_5) nanowires are also used as sensor materials in this thesis.

2.2.1. Ultra-thin Wafers and Chips

The technology readiness to obtain devices down to nanoscale dimensions and the possibility to exponentially scale the device densities up to billions of devices per cm^2, makes

silicon- based microelectronics a good candidate for addressing immediate high-performance needs in flexible electronics. For this, the first issue that needs to be overcome is the lack of flexibility (and hence conformability) of silicon wafers. This is achieved by thinning the wafers down to <50 µm using a range of technologies. Thin silicon wafers were explored initially for realizing photovoltaic arrays for space applications[18]. A detailed review on ultra-thin silicon chip technologies has been published [4] during this doctoral research. Silicon chips from such thinned wafers, or ultra-thin chips (UTCs), are ideal for high-performance flexible electronics as they are physically bendable and have a stable electronic response for a particular bending state[88]. The integrated circuits (ICs) fabricated using standard Si wafers are known to have better uniformity and stability and therefore ICs on thinned Si wafers is an attractive route for high-performance flexible electronics [91]. The excellent form factor of UTCs make their integration on flexible substrates better than the conventional thick chips. Further, due to reduced package volume and lower parasitic capacitance, the UTCs have better high-frequency performances and lower power consumption. These are the features which enables UTCs to underpin advances in areas such as sensing, computing, data storage and energy (Fig. 1-1) and several emerging applications (e.g. robotics, wearable systems, m-Health, smart cities and Internet of Things etc.).

2.2.2. Ultra-thin ribbons and micro/nanowires

In contrast to UTC, pseudo-1D structures such as ultra-thin ribbons and micro/nanowires are useful for realizing high-performance large-area electronics, (also known as macro-electronics), thanks to processes such as printing and coating [92,93,89]. Micro/nanowires in a tubular form factor could also be considered for realizing large-area electronics applications. This opens a plethora of application opportunities together with associated processing and device fabrication challenges which must be overcome. Ribbons typically have one of the dimensions several times smaller while wires have two of the dimensions smaller compared to other dimensions as illustrated in Fig. 1-2(d & e). Such, structures could be used for realizing sensors, active electronics as well as interconnects.

Nanowires are 1D structures with a diameter in the range from that of a single atom to a few hundred nano-meters and a length in the range from tens of nano-meters to several hundred microns. Nanowires demonstrate remarkable properties compared to their bulk form which finds many interesting and novel applications. There are three stages in realizing flexible electronic devices from nanowires namely synthesis, transfer printing and fabrication of electronics. All these sections form part of this thesis as presented in chapter 7. Further, the dimensions will influence not only the mechanical properties but also other physical properties such as bandgap, optical transparency etc. which could be exploited for interesting applications.

It should be noted that the use of a pseudo-1D structures-based approach for high-performance flexible macroelectronics is still at infancy, but is much needed in many applications such as drive electronics for fully flexible displays, and electronic skin etc.

2.2.3. Theoretical Background

The physical dimensions of IMNSs could influence the material properties and carrier transport mechanism and therefore could affect the performance of electronic devices. Compared to their bulk counterparts, the IMNSs may exhibit different behaviour in terms of mechanical flexibility, optical transmittance, and carrier surface mobility (e.g. upon experiencing stress) etc. These variations can be challenging to handle, for example when

one attempts to apply on IMNSs the methods and designs developed for conventional bulk semiconductors. At the same time, such variations also offer multiple new opportunities, which are otherwise difficult with bulk semiconductors.

For example, Si starts to become optically transparent for thicknesses below 10 μm - starting in the red region and progressing towards the blue region as the wafer gets thinner. Such thinning-led variations in the optical transparency of Si could be exploited to improve photodetectors and solar cells etc. The various properties are discussed with reference to ultra-thin silicon, initially, followed by special attributes of nanoribbons or nanowires.

2.2.3.1. Mechanical Properties

When a load is applied on a solid material it will deform. The deformation can be called elastic if the material returns to its original shape after the load is removed. Young's Modulus or Elastic Modulus is a measure of the stiffness of a solid material without regards to the structure or geometry of it. In the latter case where structure or geometry are also considered, the related physical parameter of measure is termed as geometric stiffness.

However, Young's modulus (*E*) also changes with thinning. While for most discussion, the Young's modulus is considered as a constant value (typically true for bulk material in the linear elastic region), it becomes thickness-dependent especially when the thickness of the material approaches the nanometer regime. This section is dedicated to a brief discussion on the mechanics of bending. Ultra-thin wafers, chips, membranes, and ribbons could be approximately studied by assuming them to be flexible elastic plates (EP). So, initially, the discussion will focus on the mechanics of an EP. Later, its implication on 1D structures, such as micro/nano-wires, is also briefly presented.

The curvature of an EP under bending strain is given by:

$$\mathbf{C} = \frac{\mathbf{1}}{\mathbf{R_C}} \qquad \textbf{(E 2-4)}$$

where R_C is the radius of curvature. It is schematically illustrated in Fig. 2-2(a, b). The higher the curvature, the lower the radius of curvature is. Fig. 2-2(c) illustrates the various components of force on an EP under bending. The dashed line is the neutral plane where the arc length after bending is the same as the length of the EP object (L) before bending. The concave side of bending experiences compressive stress with a decrease (L-δL) from the original length (L) whereas the convex bending side experiences tensile stress with an increase in the original length to L+δL. The resistance offered by a structure while undergoing bending is given by its flexular rigidity (i.e.) the force-couple required to bend a non-rigid structure to one unit of curvature[94]. The force-couple is illustrated with blue arrows on Fig. 2-2(c). The flexular rigidity of an EP is approximately given by [94]:

$$\boldsymbol{D} = \frac{\boldsymbol{Et^3}}{\mathbf{12(1-\nu^2)}} \qquad \textbf{(E 2-5)}$$

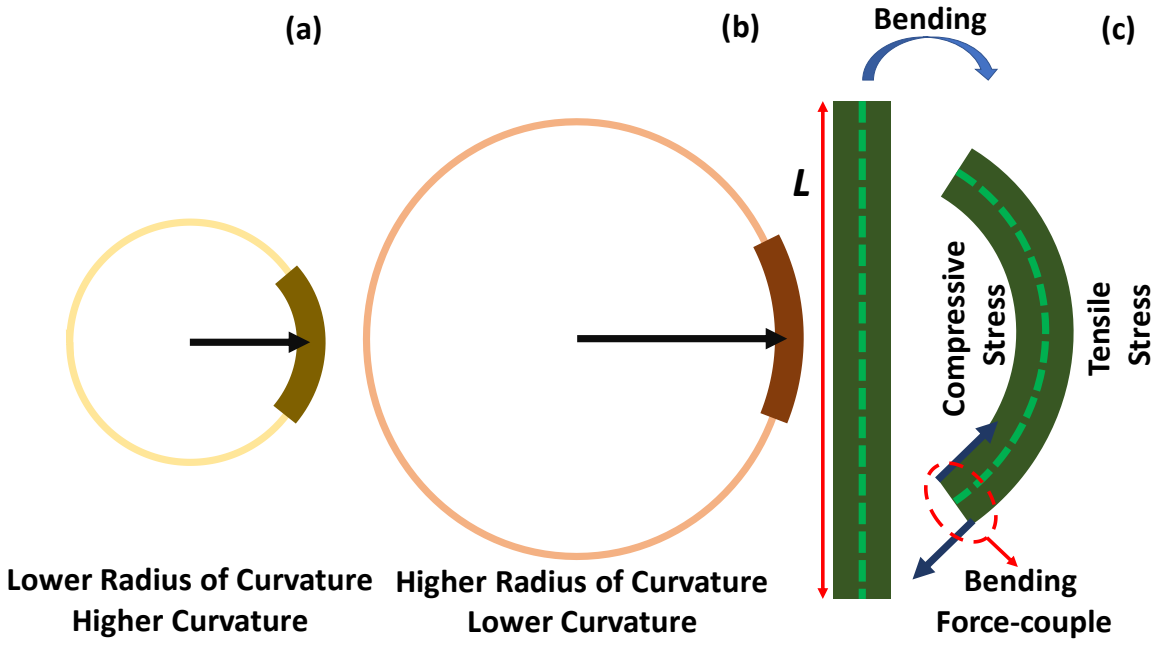


Fig. 2-2: Illustration of (a) & (b) bending radii of curvatures (c) components of force on an object under bending.

Where, E is the Young's modulus, t is the thickness of the EP and ν is Poisson's ratio. As per the equation, the flexural rigidity decreases with the cube of the thickness. This implies that more than fifteen orders of difference in flexular rigidity exist between ultra-thin Si membranes with thicknesses of 100 nm compared to bulk silicon wafers with thicknesses of 1 mm[17]. The bending strain at a given curvature relates inversely with the thickness. Both of these facts imply that at lower thickness higher bendability is possible.

The mechanical strength of Ultra-Thin chip/membrane/ribbon Structures (UTS) is also influenced by their thickness and the stress generated during the bending. Mathematically, the stress is expressed as:

$$\sigma_{st} = \frac{E*h}{2R} \qquad \textbf{(E 2-6)}$$

where h is thickness of UTS and R is the bending radius of curvature. Under bending conditions, the stress is directly proportional to the thickness of UTS and inversely proportional to the radius of curvature. The ultimate breaking strength of Si is 7 GPa[95]. This implies that for the same stress, the thinner chip will have lower radius of curvatures or can be bent more. This is also indicated by Fig. 2-3(a), where estimated values of bending strain (calculated using MATLAB code based on equations in[96]) are plotted against radius of curvature for Si with different thicknesses. The dashed line at 0.007 parallel to the x-axis indicates typical breaking strain for ultra-thin Si. However, in most cases, thin chips are packaged over flexible substrates or flexible printed circuit boards (FPCBs). In a packaged structure with UTS placed over a flexible substrate, Stoney's formula could be used to determine the stress level. In the most common form, it is written as[4]:

$$\sigma_f = \frac{E_s t_s^2}{6(1-\nu)t_f R} \qquad \textbf{(E 2-7)}$$

where t_s, t_f are substrate and film thickness, and ν is Poisson's ratio. The stress experienced by the top surface of UTS is proportional to the Young's modulus of the substrate and its thickness. For this reason, for applications requiring polymer substrates,

polydimethylsiloxane (PDMS) (E = 360-870 KPa) could be better than polyimide (PI) (E = 2.5 GPa). This is also reflected in Fig. 2-3(b), which shows ultra-thin Si over PDMS substrate that can bend up to 6 mm without breaking. As electronics are typically made of more than one layer, namely: interconnect material, field dielectric, gate conductor, gate dielectric, channel material, substrate etc., one should consider a multilayer strip while calculating the stress. Assuming the materials are elastic, approximate equations can be obtained to get intuitive results which could be further extended and used in numerical modelling.

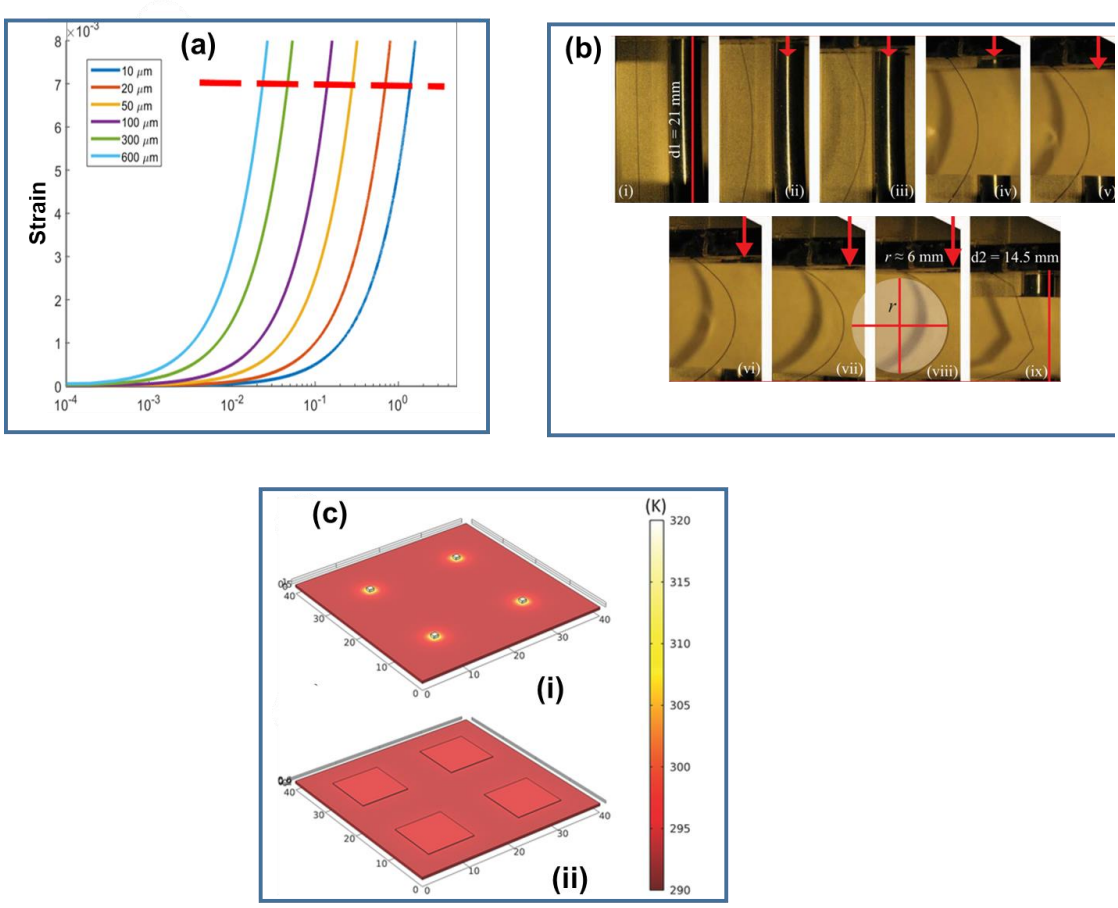


Fig. 2-3: (a) Plot showing the calculated bending strain vs. radius of curvature for various thicknesses of Si wafer (b) Bending of Si membranes on PDMS substrate showing breakage at R = 6 mm[88] (c) COMSOL simulation of heat distribution in (i) 500 µm thick chip with area 1 mm^2 showing creation of hot spots – up to 45°C for a low input power density of 1 W/cm^2[97]. (ii) 100 µm thick with area 100 mm^2, showing temperature rise of only 2°C above ambient at same power density [4] npj:CC by 4.0.

For an elastic multilayer strip with n layers, with individual thicknesses t_i, bonded sequentially, as shown in Fig. 2-4, the strain at a location y in the stack is given by [98]:

$$\varepsilon = c + \frac{y - t_b}{R_C} \qquad \textbf{(E 2-8)}$$

where, t_b is the bending axis, which is defined as the line in the cross section of the system where the bending strain component is zero and R_C is the radius of curvature. The bending axis t_b is given by the equation

$$t_b = \frac{\sum_{i=1}^{n} E_i t_i (2h_{i-1} + t_i)}{2\sum_{i=1}^{n} E_i t_i} \qquad \textbf{(E 2-9)}$$

where, t_i is the thickness of the i^{th} layer and h_i is the height at which the layer i (1 to n) is located and is given by:

$$\mathrm{h_i} = \sum_{\mathrm{j=1}}^{\mathrm{i}} \mathrm{t_j} \quad \textbf{(E 2-10)}$$

c is the uniform strain component or axial loading component on the individual layers mainly because of the contribution due to thermal expansion and is given by:

$$\mathrm{c} = \frac{\sum_{\mathrm{i=1}}^{\mathrm{n}} \mathrm{E_i t_i \alpha_i \Delta T}}{\sum_{\mathrm{i=1}}^{\mathrm{n}} \mathrm{E_i t_i}} \quad \textbf{(E 2-11)}$$

The above equations are based on [98], where authors have theoretically estimated stress in multilayer films subjected to residual stresses and external bending which is similar to that in this case. The theoretical value of the critical radius of breaking curvature ($\mathrm{R_{BC}}$) can be approximately estimated by equating the strain (ε) at the extremes $\mathrm{y_{extreme}}$ (top y_{top} or bottom y_{bot}) of Si (Equation S2) to 0.7%[89], which is approximately, the maximum bending strain observed experimentally for Si thin films. This results in the semi-analytical equation for the radius of breaking curvature ($\mathrm{R_{BC}}$) given by:

$$\mathrm{R_{BC}} \approx \frac{\mathrm{y_{extreme} - t_b}}{0.007 - \mathrm{c}} \mathrm{x}\, 10^{-3}\ \mathrm{mm} \quad \textbf{(E 2-12)}$$

The synthesis/fabrication process impacts the mechanical properties of UTS. For example, during thinning by back grinding, the sub-surface damage (SSD) and deep cracks in Si result in poor bendability and eventually may lead to early breakage of UTS. Likewise, the etch pits and hillocks produced during thinning by wet etching could lead to localised stress and can decrease the breaking strength of Si.

The localised stress or stress distribution at different locations in UTS are typically studied theoretically with numerical Finite Element Analysis[99] and experimentally by Micro-Raman Spectroscopy[100]. The 3D-FEM analysis can provide an estimate of the stress at critical positions of the complex structures forming the electronic circuitry. The shift in Raman peak could provide insight into localised mechanical stresses.

The empirical dependence of Young's modulus on the thickness of Si for thicknesses less than 85.5 nm can be described as[101]:

$$E = 54.872 * t_{Si}^{0.226} GPa \quad \textbf{(E 2-13)}$$

Where, t_{Si} is the thickness of the Si in nm.

Often the neutral plane concept (dashed line in Fig. 2-2(c)) is proposed to reduce the stress experienced by the electronics on UTS. This can be achieved by laminating or encapsulating the UTS between two layers of suitable thicknesses. In doing so one could improve the bending limits, but in practical terms it is difficult to fabricate or integrate UTS in the neutral plane. Instead of minimizing or cancelling such effects, it could be useful if an alternative strategy is devised to exploit bending induced variations in the response of UTS. As an example, variations in the output of devices on ultra-thin chip/ribbons could be exploited to predict the state of bending (e.g. curvature) or the shape of ultra-thin chip/ribbons under bending conditions. This could be achieved by developing models that accurately capture the electro-mechanical variations in the response of devices on UTS. The need to model the behaviour of electronics on flexible substrates has been felt recently as reports in this field have started to appear[102].

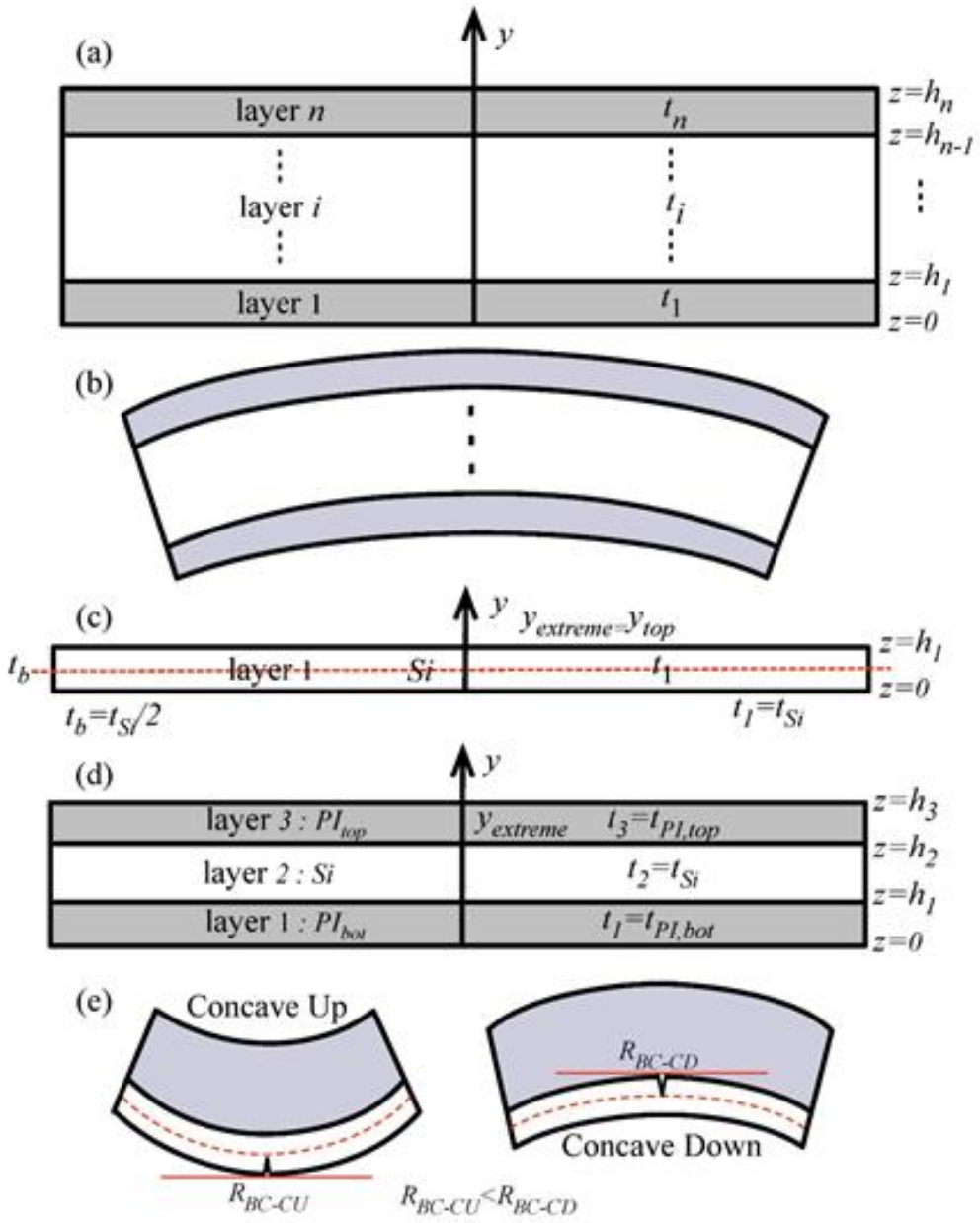


Fig. 2-4: An elastic multilayer strip with external bending: a) Stress-free multilayer film. b) the elastic-bending of a stress-free multilayer film. Structural parameters considered for finding breaking radius of curvature for c) a bare Si chip, d) Si chip encapsulated between PI layers e) Different RBC for asymmetric stacked films when bended concave up or concave down (Eg: Si/PI, Ag/SiO2/Si/PI, PI/Ag/SiO2/Si/PI, 25µm/15.36 µm / 16.48 µm PI Top/Si/PI Bot). Red solid line is the tangent to the arc forming the RBC. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

2.2.3.2. Thermal properties

Temperature is known to have significant impact on the performance and reliable operation of electronics and therefore discussion on thermal properties of UTS gain importance. It should be noted that for large area electronics from nano-ribbons or nanowires, the heat may not be a major problem because of the large area distributed electronics compared to UTCs with high density electronics. Further, the heat dissipation for UTCs realised from Silicon-on-insulator (SOI) wafers having top Si thickness in the nanoscale, significantly differ from conventional bulk Si based chips. For example, the

thermal conductivity of <100 nm thick Si is half the value of undoped bulk Si (~148 Wm-1K-1)[103]. The lower thermal conductivity implies that the heat generated is not easily transferred to the package and therefore appropriate heat management may also be needed for such UTC, especially for high-performance flexible electronics. Another important factor is the dependence of mobility on temperature, which is determined by four types of scattering (phonon scattering, surface roughness scattering, bulk charge coulombic scattering, and interface charge coulombic scattering). For example, empirically, the electron mobility (μ_{el}) in lightly-doped silicon is related to temperature (T in Kelvin) by:

$$\mu_{el} = 8.56\ x\ 10^{8} T^{-2.33}\ \frac{cm^2}{V.s} \qquad \textbf{(E 2-14)}$$

The net effect of this complex dependence is that the higher the temperature, the lower the mobility is[104] and therefore an increase in the temperature due to low thermal conductivity of UTS could degrade the system performance. Likewise, the threshold voltage decreases because the metal to semiconductor work function and fermi potential decrease with temperature[105]. The thermal issues can be overcome by incorporating on-chip cooling architecture such as micro-coolers and thermo-electric fluidic cooler[106], but may make it cumbersome.

2.2.3.3. Optical properties

Owing to varying absorption coefficients at different wavelengths, Si starts to become optically transparent as the thickness decreases - starting with the red region and progressing towards the blue region. For relatively thicker Si (>10 µm), this behaviour could be approximately explained with Fresnel equation of reflectance (Eq. 6) and Beer-Lambert's law (Eq. 7) as[107]:

$$R\ (\%) = 100\ \left|\frac{n_{Air} - n_{Si}(\lambda)}{n_{Air} + n_{Si}(\lambda)}\right|^2 \qquad \textbf{(E 2-15)}$$

$$A\ (\%) = 100\ \left(1 - e^{-\alpha_{Si}(\lambda)x}\right) \qquad \textbf{(E 2-16)}$$

where, n_{Air} and n_{Si} are the refractive indices of air (~1.00) and Si respectively, λ is the optical wavelength, α_{Si} is the absorption coefficient of Si at a given wavelength and x is the optical path length. Fig. 2-5(a) shows the optical reflectance and absorptance versus wavelength for ultra-thin Si of various thicknesses. The reflectance spectrum indicates that Si is more reflective in the blue end. Fig. 2-5(b) shows the net spectral transmittance for ultra-thin Si at various thicknesses. A noticeable difference is observed for sub-10 µm Si where it starts to become transparent in the red region. Fig. 2-5(c) shows the optical net absorptance for various depths of Si, particularly for the typical wavelengths (Blue - 475nm, Green - 510nm, Red - 650nm and Infrared - 750nm). It can be noticed that 90% intensity of these wavelengths gets absorbed within ~750nm, 1.5µm, ~7µm and 15.5µm depths. Semi-transparency can be obtained by introducing holes in the wafer using XeF_2 based isotropic dry etching and Al_2O_3 as a protective layer[108]. For applications such as photodetectors or solar cells, where higher absorptance is required along with flexibility, the optical path length in thin Si can be improved by using special optical trapping techniques such as Lambertian trapping[109,110], texturing[111], and antireflection coatings[112]. Solar cells made from thin Si with optimal surface passivation show higher open circuit voltage as in this case the photo-generated carriers can be collected effectively before they recombine. This property of varying optical transmittance with thickness could also be exploited to monitor and control the Si etching process as the thickness could be seen as a function of transmitted

light. Back thinning also contributes to achieving higher quantum efficiency in both Charge-Coupled Device (CCD) as well as Active Pixel Sensor (APS) image sensors[113]. However, their red and infrared response is decreased due to thinning. Nonetheless this could be addressed with special optical trapping techniques as described above.

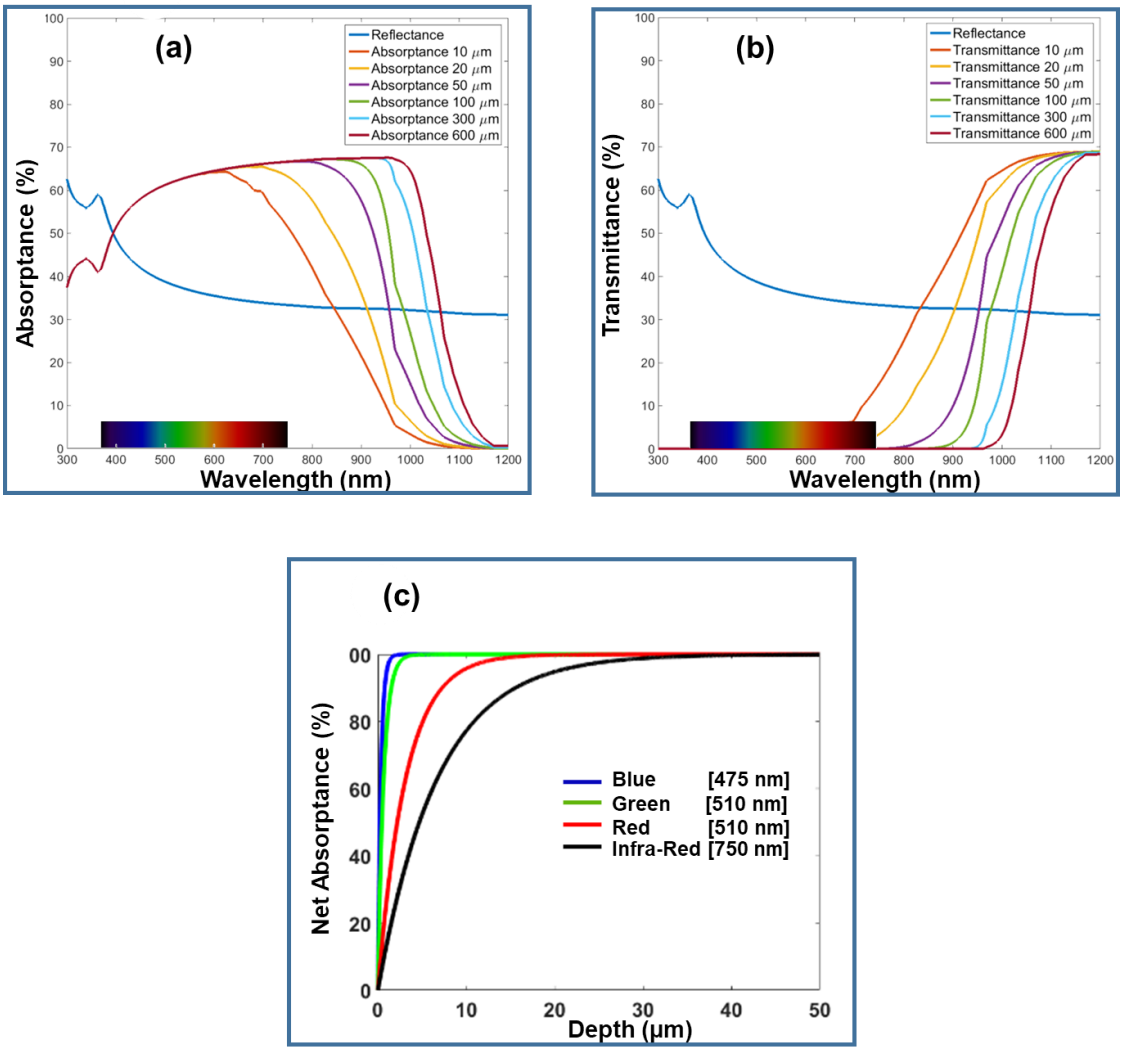


Fig. 2-5: (a) Absorptance percentage of light plotted against wavelength for different thickness of silicon (b) Transmittance and reflectance percentage of light plotted against wavelength for different thickness of silicon (c) Plot of net-absorptance versus depth for different wavelength of light. [4] npj:CC by 4.0.

In addition to the change in transmittance due to change in thickness, stress on thin Si results in bandgap narrowing (BGN). This BGN and the change in effective mass, which are related to intrinsic charge carrier concentration, can lead to an increase in the dark current of photodetectors[114]. As stated before, in addition to stress, the dimensions will influence physical properties such as bandgap of IMNS especially when the dimensions reach the nanometer regime. Diameter or Surface to Volume (S/V) ratio dependent band-gap [122] has been observed in nanowires where higher S/V ratio correlates with higher bandgap. As the band-gap changes, the optical absorption spectrum of the material changes. The band-gap-engineering of this material could find interesting applications, for example, colour-selective photodetectors were realised by using silicon nanowires just by changing the radius [115].

2.2.3.4. Electrical properties

The fundamental electrical properties of Si such as its band-gap, dielectric constant, and density of states, will not change until the thickness reaches nanoscale[116]. For most of the flexible electronics applications, the flexibility requirements could be fulfilled with UTSs having a thickness in the range of 5–50 μm. To reach <50 μm, the thickness of a conventional bulk wafer or SOI wafer undergoes a thinning process, which is known to induce stress in Si. The Si chip could also be stressed by various fabrication steps such as deposition of different material layers like oxide, dielectrics, and metal etc., which have a different elastic modulus. On top of these, there is additional stress when the UTSs are externally loaded or strained, for example, during bending. Whereas the thinning and process induced stress are intrinsic to the chip, the bending induced stress during usage is external. These stresses induce changes in the band structure and the piezo-resistive property of Si, which eventually show up as variation in the electrical response of devices on UTSs. Through electromechanical tests and modelling, a few works have attempted to capture the stress induced changes in electrical response of devices. For example, in the case of uniaxial bending in UTCs, n-type MOSFETs show an increase in mobility with an increase in bending stress. In n-type MOSFETs, this behaviour is independent of the direction of bending, but variations in the response of p-type MOSFETs is direction dependent[117]. The models in these works have taken into account the process strategies, dimensions of the structure (active Si, dielectric, metal thicknesses, etc.), initial substrate (e.g. Si, SOI, UTSOI, ETSOI etc.), mechanical strain etc. The stress induced changes could lead to deviations in the response of devices and circuits from their specified values, as can be observed from Table II, where bending induced changes in device and circuit parameters are reported. For complex circuit design in flexible electronics and to predict their response under different bending conditions precisely, it is necessary to understand these variations and implement predictive models in electronics design tools[118]. The strain generated due to mechanical bending is known to affect the band structure of the material[102]. In planar conditions, the conduction band minimum of Si consists of six de-generate Δ_6 valleys which split into two groups Δ_4 and Δ_2 under strain. Under tensile strain, the energy of Δ_4 gets lowered down with respect to Δ_2 and vice-versa for compressive strain. Similarly, tensile strain decreases the energy level of all three-valence bands and compressive strain increases their energy level. The effective mass of carrier is obtained using an E-k model either at the bottom of the conduction band or at the top of the valence band. This splitting and lowering of bands in devices under tensile stresses decreases the effective mass and the opposite happens in the case of compressive strain. Due to change in effective mass, the charge surface carrier mobility (μ) changes. Analytical equations relating the stress with the mobility and drain current[119,118] can be used to model these changes.

$$\mu_{(\text{stress})} = \mu_o\left(1 \pm \Pi_\mu \sigma\right) \quad \textbf{(E 2-17)}$$

$$V_{th\,(stress)} = \mathrm{V_{th_0}}\left(1 \pm \Pi_{\mathrm{V_{th}}} \sigma\right) \quad \textbf{(E 2-18)}$$

$$I_{D\,(stress)} = \mathrm{I_D}\left(\mu_{(\text{stress})},\ V_{th\,(stress)}\right) \quad \textbf{(E 2-19)}$$

where μ_0, I_{D0}, μ_{stress} and $I_{Dstress}$ are mobility and drain current under normal and stressed conditions respectively. The piezo-resistive coefficients Π_μ and Π_{Vth} account for sensitivity towards stress and σ is the magnitude of stress. Generally, one-dimensional descriptions of electron and hole transport in crystalline structures are used to explain the large piezoresistive coefficients observed in semiconductor under strain. The models are based on

bandgap energy models, wave mechanics, and quantum effects with dependency on dopant type, doping concentration, temperature, crystallographic direction, and relation between the current and stress direction [120]. They can also be modelled by empirically-measured first order piezoresistive coefficients (FOPR): the longitudinal π_{11}, the transverse π_{12}, and the shear π_{44}[121,122].

Table 1: First order piezoresistive coefficients [10^{-10} Pa^{-1}] for Silicon [121,122].

FOPR [π_{ij}]	p-Type		n-Type	
	Smith	**Matsuda**	**Smith**	**Matsuda**
π_{11}	0.7	-0.6	-10.2	-7.7
π_{12}	-0.1	0.1	5.3	3.9
π_{44}	13.8	11.2	-1.4	-1.4

The piezoresistive effect of MOSFET depends on the alignment of the device to the crystal orientation. For devices aligned with the <100> crystallographic direction, it depends only only to the shear coefficient π_{44} whereas for the ones aligned with <110> it is related to longitudinal π_{11} and transversal π_{12}. For p-type silicon, π_{11} and π_{12} are negligible compared with π_{44}, while FOPRs have an opposite behavior for n-type. In n-MOSFETs, the channel is n-type where the resistance decreases, and gate oxide capacitance increases with tensile bending. This means the tensile strain leads to overall increase in the current and the opposite happens for compressive strain. Performance of FETs under bending, along with results from modelling, are presented along with empirical results in chapter 5 of this thesis[123,102,124]. The variations in device response could be reduced by using suitable compensation techniques in the layout. On the other hand, these changes in the device parameters could also be seen as the signature for a particular bending state and therefore could be used to predict or sense the state/shape of bending.

Table 2: Change in device and circuit parameters realised on UTC under bending condition [4]

Device/Circuit	**Chip thickness [µm]**	**Bending radius [mm]**	**Evaluated Parameter**	**% Change**	**Ref.**
NMOS, PMOS	15	20	Drain current	~ 6	[118]
Inverter	40	15	Avg. propagation delay Midpoint voltage	~ 7 ~ 2	[125]
NMOS Current mirror	20	30	Output current	~ 5	[117]
Memory	40	5	Remnant polarisation	--	[126]
Ring Oscillator	20	25	Output frequency	~ 1.15	[127]
Comparator	20	25	Standby current	--	[127]
Ring Oscillator [SOI]	0.006	6.3	Stage delay	--	[128]

The surface of the semiconductor is a discontinuity in the periodic crystalline lattice structure where the electrical properties differ compared to the bulk. In nanoscale, the surface defects can have significant influence on the electrical properties of the whole structure.

These were exploited to realize high-sensitive sensors [129] as well as high-performance transistors [130]. Furthermore, the S/V ratio dependent band-gap [129] have influence on the electrical properties, especially the subthreshold response or leakage current of the transistors.

2. 3. Fabrication/Synthesis of IMNSs

2.3.1. Technologies for Realizing Ultra-thin Wafer and Chips

A wide range of technologies have been explored for realizing Ultra-thin wafers and UTCs. The discussions about them are given in a few review articles[120, 121] as well as the review article published during this doctoral research [4]. Fig. 2-6 gives a summary of these technologies, classified based on the fabrication stage at which the thinning is carried out. The method used during this doctoral research is anisotropic wet-etching based thinning of silicon wafers as explained in chapter 5.

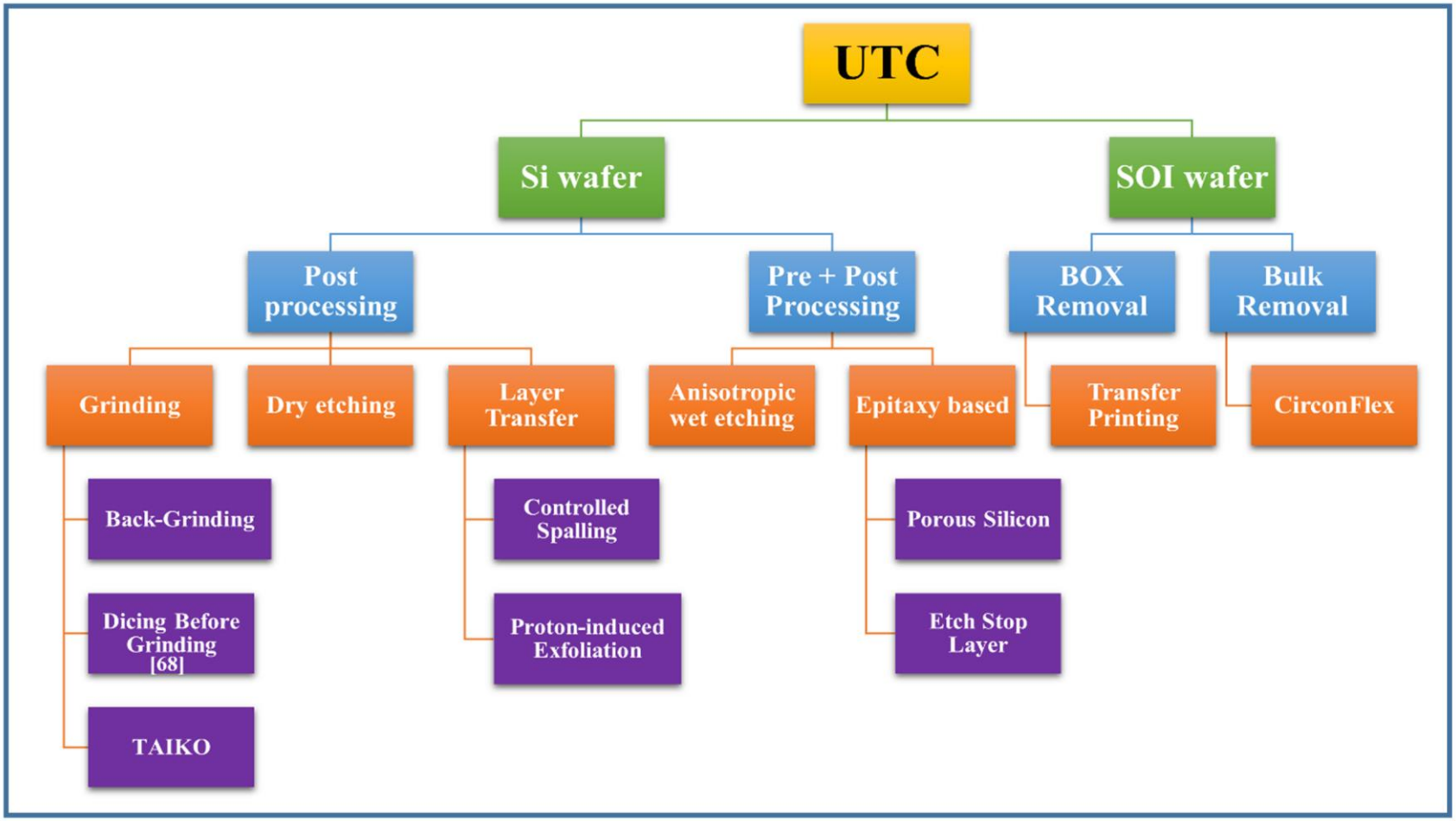


Fig. 2-6: Classification of various thinning methodologies for realizing ultra-thin silicon wafer and chips [4] npj:CC by 4.0.

2.3.2. Fabrication of Nano-ribbons

Fabrication/synthesis strategies of nanostructures are primarily divided into top down or bottom up approaches. In the case of former, one or many step(s) of removal process(es) is/are carried out on a bulk semiconductor to achieve the desired nano-dimensional structure. In the case of the latter, additive processes are used on a random or a templated assembly to obtain the nanostructure. This is also applicable to nano-ribbons which are fabricated/synthesised either using top down approaches (either from SOI wafer[131] or bulk silicon wafer [132]) as well as bottom up approaches[133]. In this thesis, top down strategies are used for realizing nanoribbons from SOI wafer as a proof of concept for demonstrating new device concepts as explained in chapter 6.

Nano-ribbons can be fabricated from SOI wafers by using a photolithographic definition of patterns followed by etching the desired ribbon structure. Flexible as well as stretchable structures[13,17] can be realised by this approach. The oxide in the SOI is used as a sacrificial layer to release the ribbons from the wafer. Such released ribbons are flexible and can be transfer printed to the desired target substrate. A similar process is explained in detail in chapter 6.

However, the cost associated with SOI wafers and use of only the top silicon layer for realizing high-performance flexible electronics is acceptable for speciality applications where higher control is required, but not for macro-electronics. In this regard, realizing nano-ribbons from bulk silicon wafers is attractive. This has been achieved by using low cost <111> bulk silicon wafers [132]. Fig. 2-7 shows the method used for realizing nano-ribbons from a <111> silicon wafer. Following lithographic patterning, SF_6 plasma etching is carried out to realize trench structures (1 µm deep x 1 µm wide). Then the etch masks are removed and thermal oxidation is used to grow 100 nm thick oxide layer on the wafer (Fig. Fig. 2-7b blue). Angled electron beam evaporation is used to deposit Ti/Au in the trench sidewalls. This angle determines the extent of "shadowing" and hence the thickness of the ribbon being etched. Finally, anisotropic etching solution of potassium hydroxide, iso-propyl alcohol and water with H_2O:KOH:IPA (3:1:1**)** is used to etch at 100˚C and undercut thereby forming freestanding ribbons. Then the Ti/Au masks are removed leaving behind the freestanding ribbons which can be used for large area applications. Back-gated thin film transistors were realised using this approach[132].

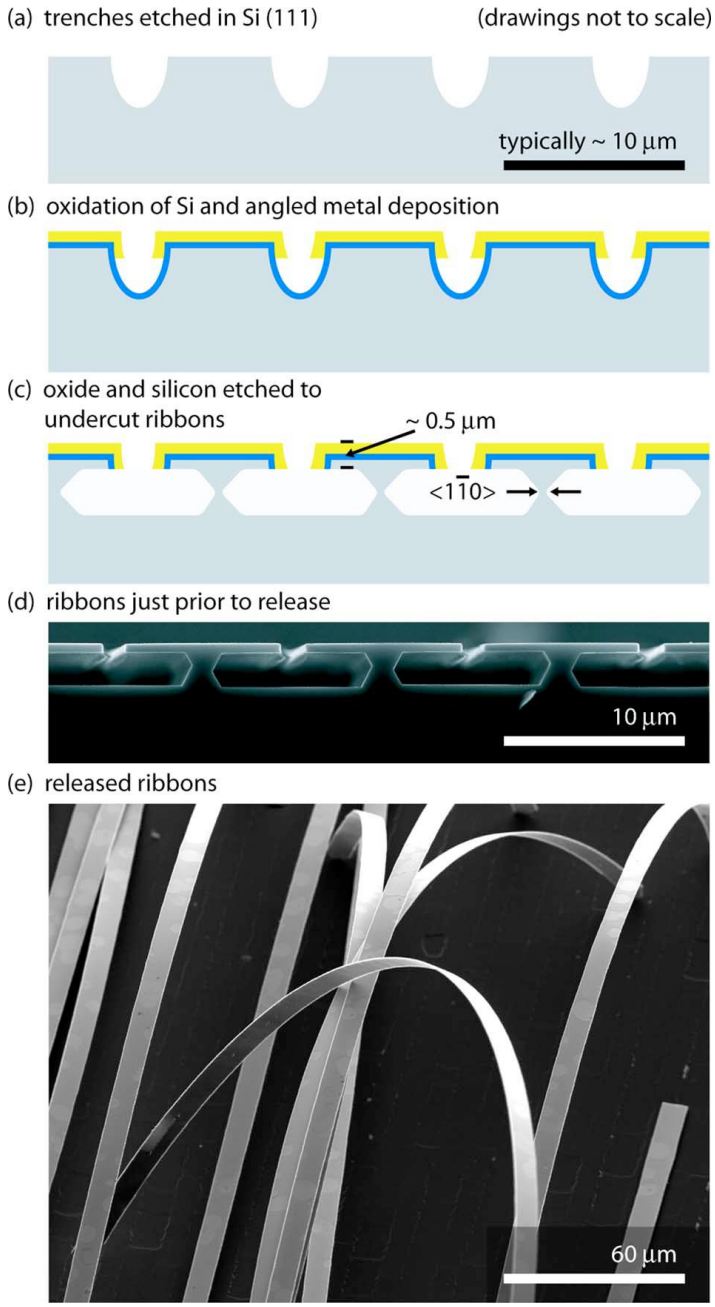
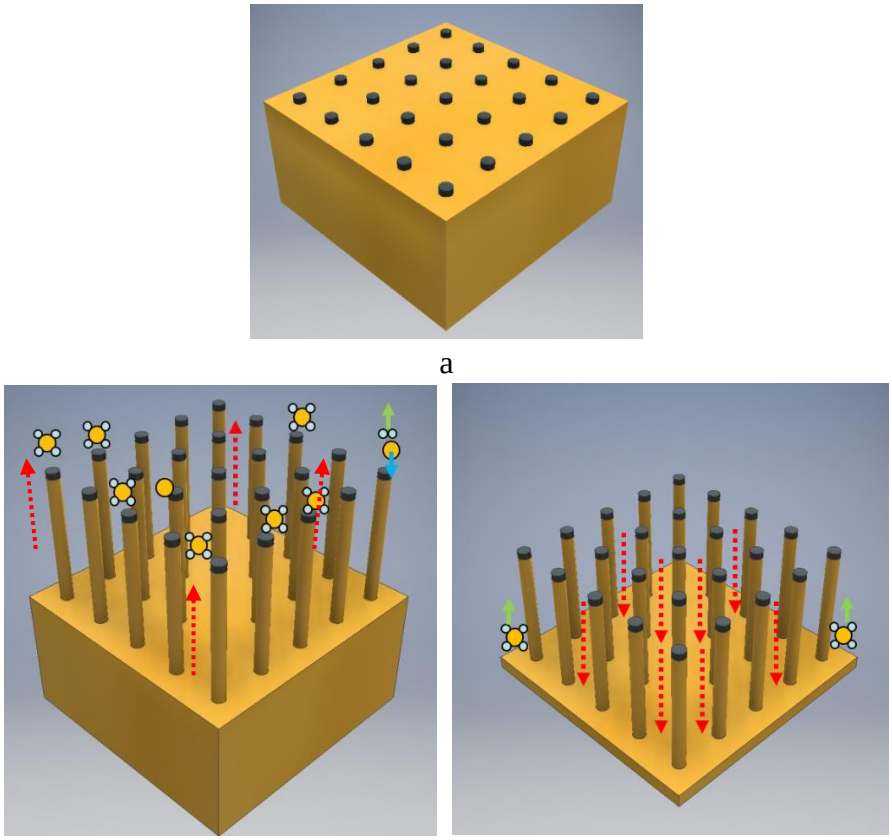


Fig. 2-7: Schematic process flow of single-crystal silicon ribbon fabrication. (a) SF6 plasma etch trenches in a <111> Si surface. (b) Thermal oxidation and angled evaporation of Ti/Au passivate the sidewalls. (c) Hot KOH/IPA/H2O solution undercuts the Si ribbons. (d) Cross-sectional SEM image of partially undercut ribbons. (e) Released, flexible ribbons. [132] Reprinted from Applied Physics Letters, vol. 88, pp. 213101-3, 2006, with the permission of AIP Publishing.

2.3.3. Fabrication/synthesis of nanowires

The fabrication of nanowires (illustration in Fig. 2-8) can be summarised into two important stages as given in Table 3: namely the patterning stage and the growth/etching stage. While some of these processes could also be used for synthesizing microwires, the focus is given to nanowires. Depending upon the second stage, the overall process may be called either a bottom-up approach or a top-down approach. If growth is involved it may be termed as bottom-up, while, if etching is involved it may be termed as top-down [134].



a b or c

Fig. 2-8: Illustration of fabrication of Si NWs a)Nanopatterning b)Growth or c)Etch

Stage 1: Nanopatterning

There are various possibilities to achieve patterning for nanowire fabrication. The patterning could be direct nano-size patterning as is possible with e-beam/Ion Beam lithography, or formation of micron-sised features with photolithography and then further reducing/shrinking the dimensions to the orders of nanometers. Both horizontal nanowires as well as vertical nanowires can be formed by proper choice/combination of substrate, stage 1 and stage 2 techniques (summarised in Table 3).

Stage 2: Growth/Etch

As stated before, this stage can be divided into two sub-types based on the processes involved

a) Etch/Top-down Approach:
b) Growth/Bottom-up Approach:

Table 3: Fabrication of Nanowires

	Top down/Etching				**Bottom-up/Growth**					
Stage 2 / Stage 1	Metal Assisted Chemical Etching (MACE)	Deep Reactive Ion Etching (DRIE)	Reactive Ion Etching (RIE)	Stress Dependent Oxidation/ Wet Etching	Vapour-Liquid-Solid (VLS)	Supercritical fluid−liquid−solid (SFLS)	Supercritical fluid−solid−solid (SFSS)	Solution−liquid−solid (SLS)	Vapor-solid-solid (VSS)	Oxide assisted growth (OAG)
Random/statistically distributed/self-assembled patterns /seeds or self-seeded	[135] [136,137]				[138] [139] [140]	[141]	[142] [143]	[144]	[145]	[146]
Template Assisted	[147]				[148,149]			[150]		
Nanosphere assembly/lithography	[151]				[152]					
E-beam Lithography		[153]			[154,155]				[156]	
Ion Beam Lithography										
X-ray Lithography										
Photolithography	[157]			[158]	[159,160]					
Interference Lithography	[161]				[162]				[163]	
Extreme UV Lithography										
Immersion Lithography			[164]							
Soft Lithography	[137]				[165]					
Spacer lithography or Self Aligned Double Patterning (SADP)			[166]							
Nanoimprint lithography	[167]				[168]					
Superionic Solid State Stamping (S4)	[169]									

2.3.3.1. Etch/Top-down Approach

The top-down approach starts with patterns of micro/nano-dimensions and further etching it to form necessary nanostructures as shown in Fig. 2-8. The various techniques available to fabricate nanowires using top-down approach are given in the first row of Table 3.

2.3.3.2. Growth/Bottom-up Approach

The bottom-up approach involves growth of nanowires where atomic/molecular species (Eg. SiH_4) are allowed to self-assemble/crystallize on a statistically distributed or well-defined template to form nanowires, as illustrated in Fig. 2-8 and Fig. 2-9. The by-products of the reaction escapes the crystallisation zone (Eg. H_2). Bottom-up assembled nanoscale electronics are very promising for large area electronics and have potential applications in realising novel architectures. The fabrication strategies differ significantly compared to the top down approach.

2.3.3.3. Examples of strategies to synthesize nano-wires

Metal de-wetting followed by vapour-liquid-solid (VLS) epitaxy

The most commonly used method for nanowire growth widely studied in literature uses a combination of metal de-wetting and vapour-liquid-solid epitaxy as illustrated in Fig. 2-9.

Stage 1: Statistically distributed nano-patterning by metal de-wetting:

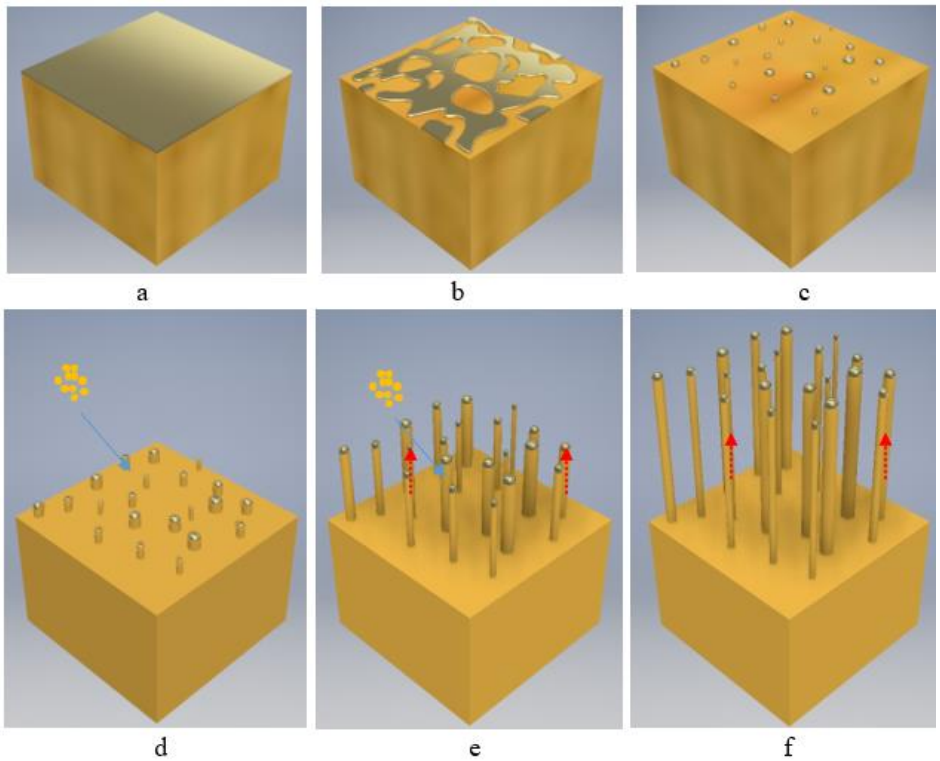


Fig. 2-9: Illustration of metal de-wetting followed by VLS for the growth of Si NWs (a-c) Stage 1:Statistically distributed nano-patterning by metal dewetting. (d-f) Stage 2 (VLS Growth of nanowires)

In this method, an ultra-thin layer of metal is deposited through physical vapour deposition (PVD) technique. When this layer is heated above the eutectic point temperature, the continuous film will become liquid and break into small liquid droplets of different

diameter depending upon the process conditions as shown in Fig. 2-9 (a to c). The eutectic point is a temperature/pressure combination where solid, liquid, and gas phases all co-exists in the phase diagram.

Stage 2: VLS Growth

The Vapour-Liquid-Solid (VLS)[170] growth technique is the most studied technique of nanowire growth. Many metal catalysts such as aluminium, nickel, titanium, zinc, tin, indium, and gold can be used as a catalyst and patterned in stage one. Gold has been the most widely used as a catalyst. The catalyst is introduced to direct and confine the crystal growth in a specific orientation and within a confined area. In this example the nano-islands of gold/silver/any other metal formed on stage 1 will act as a catalyst. The catalyst islands are heated to the eutectic point which forms a liquid droplet by itself. These islands act as a trap for growth species. The growth species are introduced in the gaseous form followed by elemental dissolution into a liquid droplet. Nanowires precipitates at the interface between the substrate and the liquid [171,140].

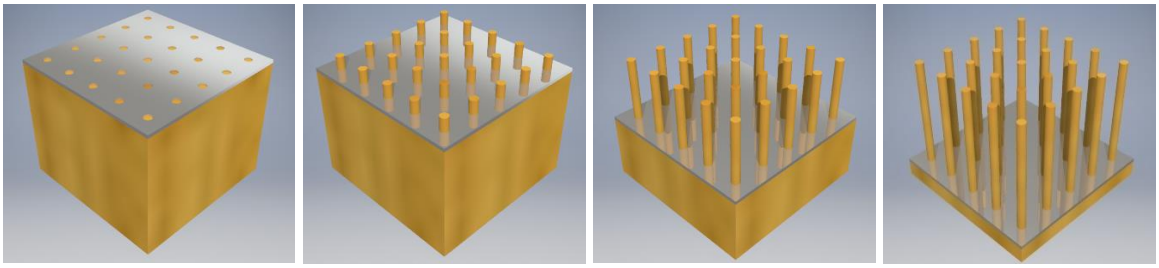
The VLS mechanism can be combined with various nanopatterning techniques. This approach has been used to synthesize SiNWs with diameters between 10 and 110 nm by varying evaporated Au layer thickness on Si wafer between 1 and 5 nm during dewetting [138]. SiNW diameter can also controlled through temperature, annealing time and Au layer thickness, with an increase in the layer thickness resulting in increase in SiNW diameter as well as density[138].

The VLS can be achieved in a variety of deposition systems such as

- Pulse Laser Deposition (PLD)
- Thermal Evaporation
- Molecular Beam Epitaxy (MBE)
- e-beam evaporation
- Laser Ablation
- Metal Organic Chemical Vapor Deposition (MOCVD)
- Atmospheric Pressure Chemical Vapour Deposition (APCVD)
- Low Pressure Chemical Vapour Deposition(LPCVD)
- Plasma Enhanced Chemical Vapor Deposition (PECVD)
- Pulsed PECVD

Nano-patterning followed by Metal Assisted Chemical Etching (MACE) for fabricating Silicon Nanowires

MACE is one of the promising route for fabricating semiconductor nanowires with controlled diameter, length, density, structure, orientation and doping [172] which are prerequisite to realize high-performance flexible electronics. It is a simple and low-cost method for fabricating semiconductor nanowires. In this method (illustrated in Fig. 2-10), a semiconductor substrate is patterned with a nano-mesh-like metal structure comprising of a noble (Ag, Au or Pt) metal. It is subjected to etching in an etchant comprising of HF and an oxidative agent (typically H_2O_2). The noble metal catalyses the etching of semiconductor beneath it. Due to this rapid etching, the noble metal mesh sinks inside the semiconductor underneath resulting in the formation of semiconductor wires. Because of the simplicity, MACE is used for synthesizing silicon nanowires during this thesis as explained in chapter 7.



a b c d

Fig. 2-10: Illustration of MACE for fabrication of NWs a) A metal nanomesh is fabricated on the top of silicon wafer (b-d) the wafer is etched in a solution of HF/H2O2/H2O mixture where the metal catalyses the etching of silicon underneath resulting in the sinking of the metal nanomesh. The process proceeds until nanowires are obtained of sufficient length.

2. 4. Applications of High-Performance IMNS for Tactile Sensing

As discussed in the introduction chapter IMNSs find a wide range of applications in several areas. In terms of the scale of these applications, they can be classified into: 1) High-density micro/nanoelectronics 2) Large-area Macro-electronics.

2.4.1. Micro/Nanoelectronics Vs. Macroelectronics

1) Micro/Nanoelectronics

Thanks to Moore's law and ITRS roadmaps[173,174], CMOS technology has come a long way by overcoming many challenges with a plethora of material and technology innovation leading to the current state-of-the-art. Commercially, 14nm technology FinFET based microprocessors are available which operate at >4GHz and are now gearing towards 7 nm[175]. However, the integrated circuit chips fabricated from CMOS technology is not flexible. While they can be integrated as a rigid island element or array on flexible substrates as illustrated in Fig. 1-2f, for efficient integration onto a flexible substrate, the UTC approach will be the key as illustrated in Fig. 1-2c. This will solve several challenges associated with thermal management and mechanical mismatch compared to bulk chips as explained in the properties section.

The UTCs could form key components of various smart systems as sensing units, data processing or storage units, driving or output units and power or energy management units wherever high-density electronics is required. Depending on the application requirements, the specification of the components on UTCs may vary. In many applications such as flexible portable display devices they should be integrated with other macroelectronics component forming smart systems.

2) Macroelectronics

Micro/nanoelectronics systems have been primarily driven by innovations that aid in reducing the critical dimensions of the fundamental building block mainly the pitch of the array of the transistors. This scaling is aimed to improve or increase the speed, memory, energy efficiency and computing capacity of processors. In contrast, macroelectronics, also known as large-area electronics, are distributed over a large area. Such systems can be

fabricated by approaches such as printing or coating. Applications of such systems include flexible displays, sensory skins, active antennas electronic textiles, structural health monitors, conformal X-ray imagers, and energy harvesters[13,86,1,90,34]. Inorganic flexible structures such as ribbons and wires could find application in macroelectronics.

IMNSs could form functional components for flexible microelectronics, macroelectronics as well as hybrid electronics. Electronic skin is one example of such hybrid electronics where a combination of both IMNS-based both flexible microelectronics as well as macro-electronics is desired because of the stringent application specifications. Specific components of various other smart micro/macro/hybrid-electronic systems where IMNS structures can be used are discussed in detail in the published review [4] divided into:

1) Sensing/Input
2) Data Processing/Storage
3) Driving/Output
4) Power Management and Energy Harvesting

With view of the above, IMNSs technology appears promising for many emerging and futuristic application especially in the area of flexible electronics. Since, the major application of this thesis focuses on tactile sensitive electronic skin, the forthcoming sections elaborates on how IMNSs could be useful to advance tactile electronic skin.

Touch panels which are widely used could be considered as a rudimentary form of e-skin. By measuring the change in resistance, capacitance, optical, mechanical, charge or magnetic properties of the material being touched, the act of touch can be detected. Based on this there are various types of touch-screens namely resistive, capacitive (self and mutual), acoustic and optical [44]. Resistive touch screens majorly work in single-finger touch mode and need complex designs/architectures for implementing multi-touch – at a significantly high cost. Air gaps that must be maintained in resistive touch screens could lead to false inputs in flexible layers and hence cannot be used for bending applications. Capacitive touch screens allow multi-touch operations; but at the expense of increased per-cycle readout time. Other touch-screen technologies such as acoustic touch screens and infrared touch screens suffer from ambient light interference and are sensitive to liquids and contaminants.

Portable devices such as smartphones are expected to be flexible in the future, and for this to happen various components including touch panel should be flexible. In such cases, the active tactile layer could comprise of large area flexible macroelectronics made of inorganic ribbons or wires or thin films[14,34,33], but the sensory data from the array of taxels can be processed locally by a tactile interface microelectronic UTC before the data is transferred to complex computing hardware. The technology discussed in this thesis for tactile e-skin could find application in realizing flexible touch panels for future portable devices [176]. In this thesis, ITO on poly ethylene terephthalate(PET) sheet were used to realize passive matrix flexible tactile skin. Active elements was also realised and tested as presented in later chapters. UTCs will strengthen the capability of such systems by enabling features that require high-performance such as multitouch sensing, 2D/3D gestures, handwriting recognition, pen/stylus input, pressure sensitivity, fingerprint recognition, and security operations thereby reducing the load of the computing block.

2.4.2. Human Tactile Sensing

Humans and other biological organisms use tactile feedback to interact with the environment [177]. Inspired by nature, numerous research groups are harnessing the technological advances to develop artificial electronic skin (e-skin) with features mimicking the human skin [34,178,179,46,180-182]. These works find application in prosthetics, to potentially bestow lost sensory feelings to amputees [183] and in robotics, to provide the touch sensory capability allowing them to interact physically and safely with real-world objects [43]. Both these applications are discussed below and are followed by a discussion on schemes and specification of electronic skin. Thus far, the major focus of artificial skin research has been on the development of various types of sensors (e.g. contact pressure, temperature, etc.) and their integration on large and flexible or conformable substrates [184,178]. In order to design an efficient tactile sensitive neuro-prosthetic system, it is vital to understand how tactile sensing works in biological systems [177].

In humans, the skin area can be divided into glabrous and non-glabrous areas and each of them have different types of sensory receptors.

The glabrous (hairless) areas of the human skin comprise of four main types of mechanoreceptors namely: Meissner corpuscles, Pacinian corpuscles, Merkel cells and Ruffini corpuscles, also schematically illustrated in Fig. 2-11. Meissner corpuscles (FA-I) and Pacinian corpuscles (FA-II) come under Fast adapting (FA) mechanoreceptors (i.e.), they fire bursts of action potentials (AP) during the onset and offset of various tactile stimuli but remain silent during steady state. They are also known as rapid adapting (RA) mechanoreceptors. Merkel cells (SA-I) and Ruffini corpuscles (SA-II) are slow adapting (SA) mechanoreceptors. Both static and dynamic sensors are needed to mimic biological tactile sensors. Merkel cells and Meissner corpuscles are closer to the surface of the glabrous skin with a smaller receptive field (<3 mm) whereas, Ruffini and Pacinian corpuscles are deeper in the skin and have a larger receptive field. Table 4 summarises the various receptors in the glabrous area of human skin and their functionalities. SA-I are useful for sensing fine details and for discrimination of object shape and textures. FA-II can also help in

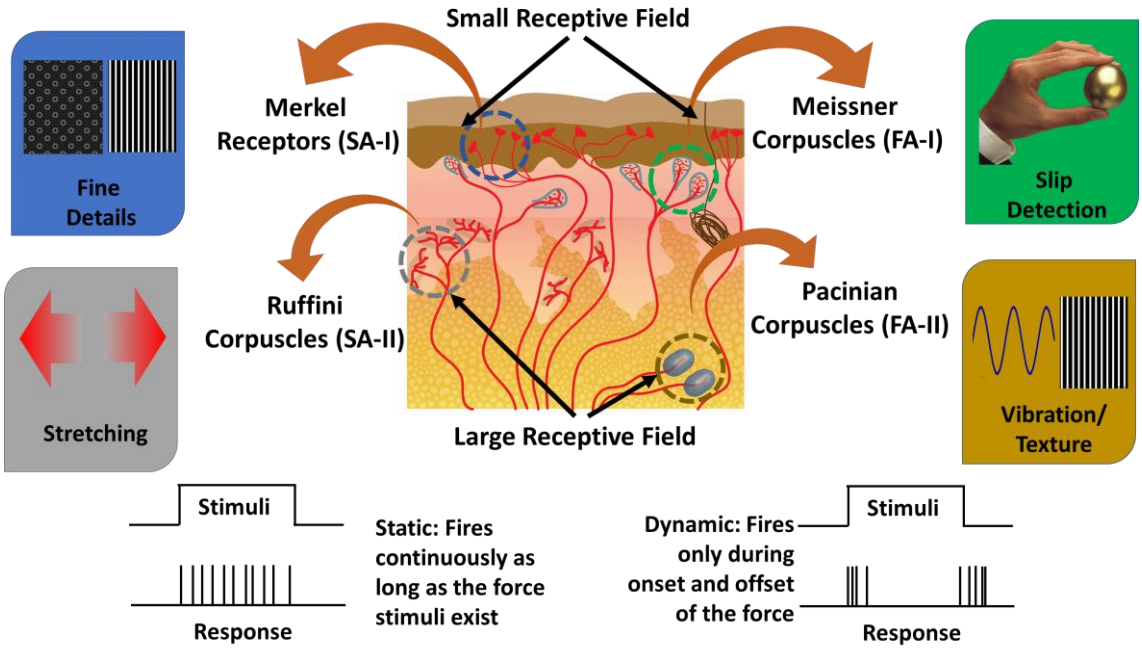


Fig. 2-11: Mechanoreceptors in glabrous area of human skin.

discriminating object textures with aid from the sliding motion of the fingers against the object's surface. Fingerprints have been found to play a key role in tactile perception of fine textures (spatial scale <200 micrometers)[185]. In this thesis, approaches carried out for realizing both static and dynamic sensing are discussed.

Table 4: Mechanoreceptors in human skin and their functions

Sense Receptor	Function	Reference
Mechano-ceptors Slow Adapting SA-I or Merkel corpuscle	Innocuous mechanical stimuli (Static forces, very sensitive, high resolution, sensing fine details, useful for discrimination of object shape and texture, receptive field size ~2-3 mm)	[186-189] [24]
Mechano-ceptors Slow Adapting SA-II or Ruffini corpuscle	Innocuous mechanical stimuli (Static forces, skin textures, proprioception, receptive field size ~10-15mm)	[186,187]
Mechano-ceptors Fast Adapting FA-I or Meissner corpuscle	Innocuous mechanical stimuli (Dynamic forces and vibrations, low-frequency (5–50 Hz), object manipulation, texture discrimination, slip detection, controlling hand grip, receptive field small)	[186,187,190,24]
Mechano-ceptors Fast Adapting FA-II or Pacinian corpuscle or Vater-Pacinian corpuscles or Lamellar corpuscles	Innocuous mechanical stimuli (Dynamic forces and vibrations, measure high-frequency vibrations (up to 400 Hz), slip detection, fine texture when figure moves, receptive field very large)	[186-188,185,190]
Noci-ceptors	Polymodal (Noxious cold, noxious heat or more than one noxious stimulus modality)	
Warm Thermo-ceptors	Innocuous thermal Stimuli	[191]
Cold Thermo-ceptors	Innocuous thermal Stimuli	[191,192]
Combination of mechanoceptors and Proprioceptive sensors (muscle spindles and fibrous capsules, partly from SA-II)	Hardness, Joint positions in space	[193]
Combination of mechanoceptors (SA-I, FA-I, FA-II, SA-II) and thermoceptors	Wetness	[194]

Another important factor to consider is the density and the number of mechanoreceptors in the human skin. This is needed to find how sensors have to be distributed, read-out and hierarchy planned for a full-body robotic skin in par with human. Also the density and the sensor count will set what technology should be used for realizing electronic skin at different parts of the robot[43].

Fig. 2-12 shows that an estimated 45k mechanoreceptors are distributed across ~1.5m^2 area of human skin, based on reports in the literature [195,24,196,197]. Out of 45k receptors an estimated ~21k sensors are in each upper limb area - mainly concentrated on the glabrous

skin of the upper limb (~18k sensors). This is an estimate of only mechanoreceptors, and the number of sensors will be much higher if we consider that tactile sensing also involve thermo-receptors and nociceptors [24] responsible for sensing temperature and pain. With the recent shift in the focus of tactile skin research in robotics from hands to whole-body tactile feedback, a need has risen for new techniques to manage the tactile data. Currently, limited solutions are available to deal with large data generated in tactile skin. In case of prosthesis, it is important not only to collect the tactile data for critical feedback, but also to decode the user's intentions in real time [183]. For this, neuron-like inferences early on from the tactile data, thus reducing the data along the sensory pathway could help. A significant downstream reduction in the number of neurons transmitting stimuli is observed in early sensory pathways in humans [198-200]. Research suggests that within the biological tactile sensory system, distributed computing takes place [177]. The distributed local processing of tactile data allowing it to be partially processed close to the sensing elements and sending the smaller amounts of summary data to higher-perceptual level, as in biological skin is advantageous [44,200].The tactile related neural spikes are found to have locally encoded information of the force's magnitude, direction and the local curvature [186,201]. In this regard, the hardware implemented neuromorphic tactile data processing along with neural networks like algorithms within the e-skin could be helpful and may have many advantages. The key challenges in realizing e-skin are: (1) distributed multi-sensors (2) processing of large data distributed over a large area and (3) encoded data transfer to higher level.

IMNSs based flexible electronics could be used for realizing neural mimicking e-skin. A sample implementation scenario and further futuristic directions are presented in the final chapter of this thesis involving the concept of neural nanowire FET(ν-NWFET).

2.4.3. Robotic Tactile Sensing

CNTs, organic polymers, graphene, and silicon are typical material technologies used by various researchers for making e-skin elements [43][34,202]. Despite the wide spectrum of sensors currently available as listed in **Table 5**, touch sensing has not been widely implemented both in prosthetic and robotic platforms. Although the concept may seem futuristic, research on electronic skin has wide-ranging practical impact. The challenges associated with tactile sensing are the distributed nature of sensors and hence the computations, the requirement for bendability, the varying spatiotemporal resolutions required at different parts of the body, and the need to detect multiple contact parameters [203,44]. A solution which addresses all these issues does not exist as of yet. The IMNSs based flexible electronics technology could help in addressing these challenges. For example, UTC technology could find application as an e-skin element for prosthesis or robotics (a flexible and transparent electronic skin for sensing/input as illustrated in Fig. 1-1a)[34,178,177,43] especially in areas to mimick tactile sensing in fingertips. In order to achieve biomimetic tactile sensing, about 250 MRs/cm^2 (plus additional thermoceptors- and nociceptors-equivalent) are required in the fingertip of a prosthetic limb[42], which could be achieved by high density tactile sensors such as flexible Piezoelectric Oxide Semiconductor Field Effect Transistor (POSFET) that can conform to fingertips[204] (Fig. 2-12). For areas where a lower density of tactile sensors is required, an IMNS based macroelectronics strategy is useful [205]. Some of the prior implementations of materials used for tactile sensing are summarised in Table 5 compared to the glabrous area of human skin. A review paper of various materials useful for tactile sensing has been published during this doctoral research[46].

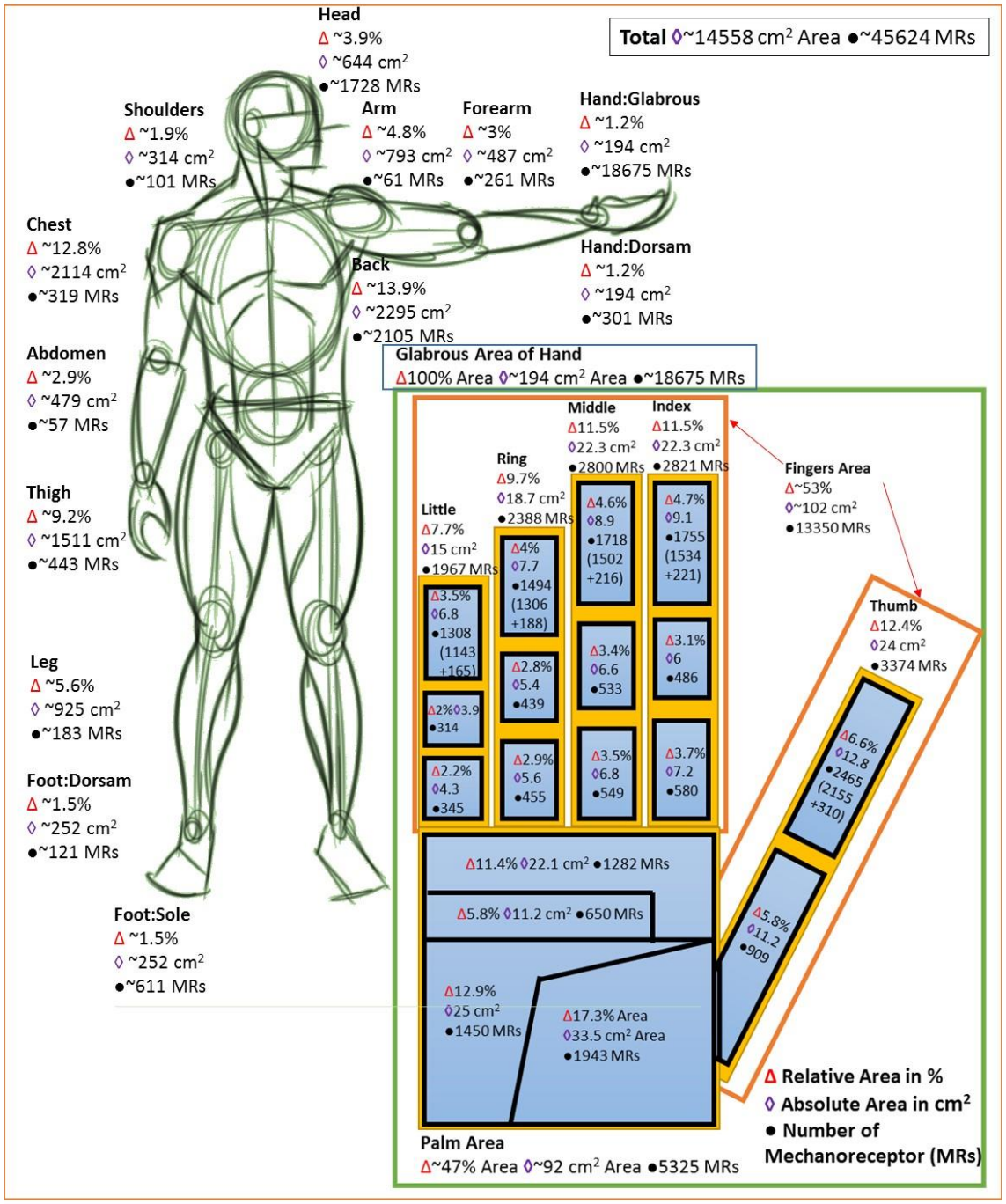


Fig. 2-12: The estimated distribution of mechanoreceptors in various parts of human skin. [33]. Frontiers:CC by 4.0.

IMNSs in the form of FETs can contribute in making both dynamic and static sensor arrays. The POSFET is an example of a dynamic sensor that can mimic FA-I and FA-II where, in its implementation a silicon-based field effect transistor is used [41] as a sub-element. In case of the POSFET, a piezoelectric material is used over the top of a MOSFET gate as shown in Fig. 2-13 (a). Akin to FA mechanoreceptors in human skin, the POSFETs are capable of sensing and (partially) processing the tactile signal at the same site. There are several advantages in the marriage of sensing material and the electronics such as event driven signalling, better integration, better signal to noise ratio, faster response, wider bandwidth, better force sensitivity, and no interconnect is required between transducer and electronic devices [206,41]. Further, such transistors could directly form a component of an

amplifier or a higher order circuit [119]. So far, POSFETs have been fabricated using bulk silicon. Using CMOS fabrication strategy, POSFET technology could be used to fabricate high density taxels. The wafers or chips could be thinned as schematically illustrated in Fig. 1-2 to make them flexible. Alternatively, printing of nanowires could be used to realize a POSFET. Such devices are expected to have higher sensitivity due to higher surface-to-volume ratio of nanowires compared to silicon chips based POSFETs.

Table 5: Prior art of demonstrations of electronic skin. Adapted from [207]

Technology	**Sensor Density cm-2**					**Mechanics**	**Ref.**
	Temp -erature	Pres s- ure	Strain	Dynamic Forces	Humidity		
Human fingertips	4	70	48	163	Intra- sensory interaction	Stretchable, durable, self-healing, bio-degradable, neural architecture	[195] [208]
Human Palm	4	8	16	34	Intra- sensory interaction	-do-	[195] [208]
Carbon Nanotubes (CNT)	-	25	-	-	-	Stretchable	[209]
Self-healing sensor	-	1	-	-	-	Self-healing	[210]
Bio-degradable Polymer	-	13	-	-	-	Biodegradab le	[211]
Stretchable Silicon	11	44	44	-	1	Stretchable, Nanoribbons	[131]
Piezotronic	-	846 4	-	-	-	Flexible	[212]
All-graphene	25	25	-	-	25	Stretchable	[213]
CNT active matrix	-	8.9	-	-	-	Flexible	[214]
Organic active matrix	7.3	7.3	-	-	-	Flexible	[215]
Organic Digital	-	1	-	-	-	Flexible	[216]
POSFET	-	-	-	100	-	Rigid	[41]
Coplanar Graphene	-	1	-	1	0	Flexible, Transparent, Energy Autonomous	[34]

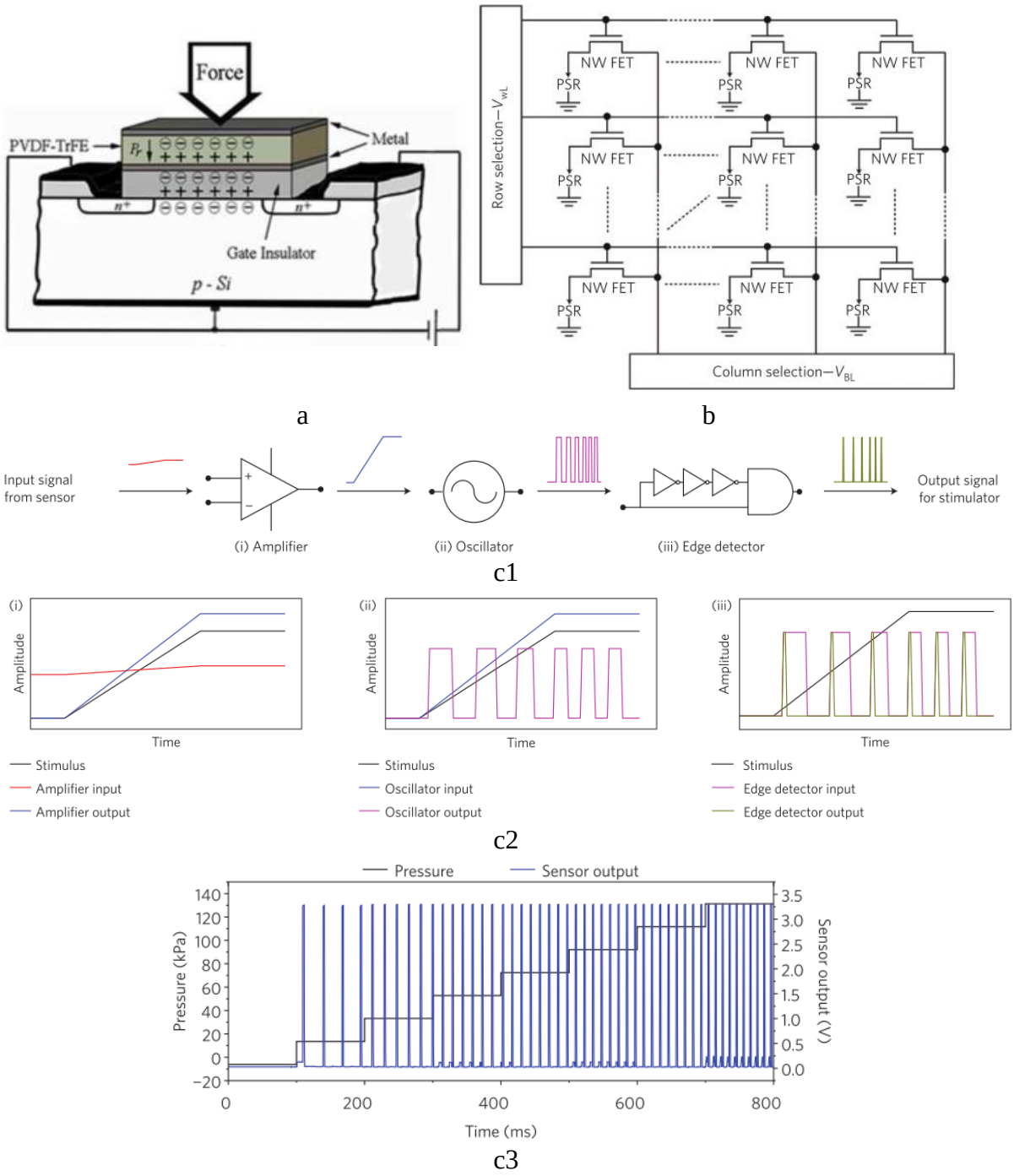


Fig. 2-13: Sensor integration strategies with inorganic micro/nanostructures FETs (a) POSFET [41] (b) Resistive Transducers [217] [218] (c) signal to spike or AP convertor for biomimetic tactile signal transducer: (c1-i to c1-iii) shows the components for the spike converter namely (c1-i) amplifier (c1-ii) oscillator (c1-iii) edge detector (c2-i to c2-iii) shows the input-output of each stage corresponding to (c1-i to c1-iii) (c3) Example spike output where the spike rate depends on the output of the sensor [216].

Fig. 2-13b shows the second strategy where inorganic nanostructures are used as active-matrix addressing elements of the sensor array. The row selectors activate the gates while the column selectors are useful to read individual sensor elements. The use of high-performance inorganic flexible FETs is promising here as the high mobility leading to low ON resistance favours a low signal-to-noise-ratio(SNR) and efficient readout. The high on-to-off ratio contributes towards lower leakage and hence results in lower power consumption and cross talk.

Fig. 2-13c shows the third strategy which involves a biomimetic signal to spike rate conversion where an IMNS-based approach could offer a high-performance highly efficient solution. The spike rate conversion is achieved by 3 components c-i to c-iii connected in series namely: amplifier, oscillator and edge detector. The amplifier is an optional component for this conversion. The transducer could be a part of the oscillator (for example a ring oscillator based on silicon nanowires) and finally connected to an inorganic nanostructured material-based invertor. Inorganic nanostructures are promising for obtaining printable highly efficient spike rate coders. Alternate innovative strategies are also possible such as the one presented in the final chapter of this thesis involving ν-NWFET.

To summarize, UTC technology finds application in realizing e-skin elements on highly sensitive and high-resolution areas such as the finger-tip of a robotic hand. A micro/nanostructures-based printing approach finds application in realizing macro-electronic skin for the rest of the robot's surface. Both, static and dynamic sensors are realizable with IMNSs which are key in achieving human-like tactile sensing in robots. In the next section the application of e-skin with reference to bidirectional prostheses are discussed.

2.4.4. Electronic Skin for Prostheses

The importance of tactile sensing in prostheses has been discussed in the introductory chapter 1. The skin technology discussed for full-body robotic tactile sensing could find application for sensing in prostheses also. However, for bidirectional prostheses interface technologies beyond tactile sensing are required where IMNS could be used, as explained in this section.

The key blocks of the electronic skin system for closed loop neuro-prosthetics (illustrated in Fig. 2-14) are:

(1) distributed flexible tactile data sensing system

(2) distributed data acquisition and processing system

(3) interface between residual limb and the prosthetics.

(4) control of prosthesis

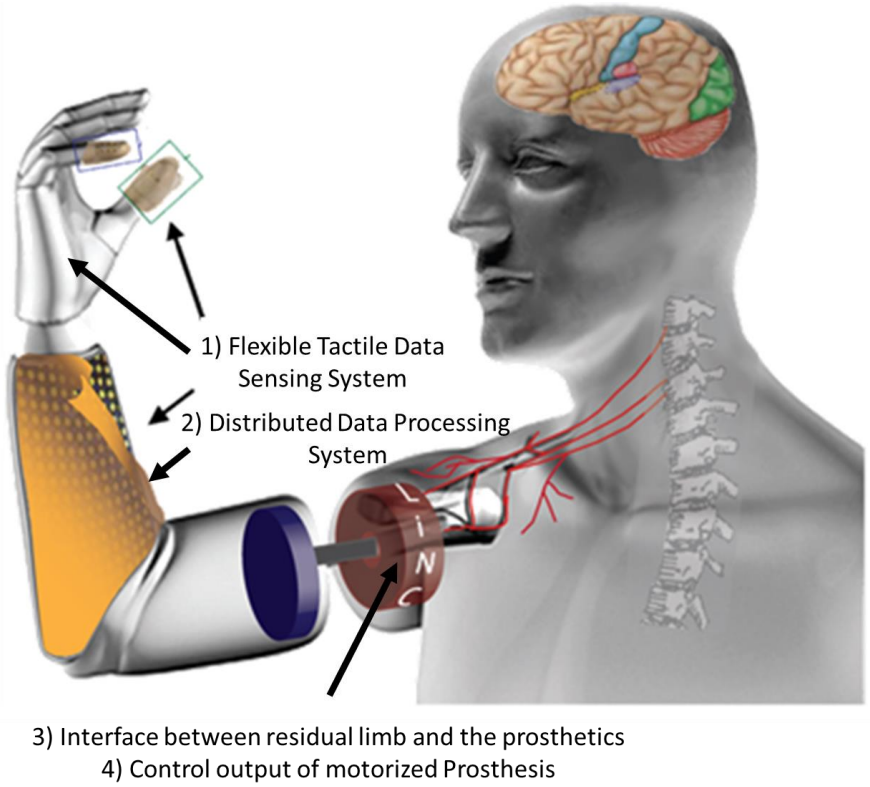


Fig. 2-14: Schematic of electronic skin system for closed loop bidirectional prosthesis [219].

IMNS-based FETs could find application in various forms at each stage for the above application. Fig. 9-2 depicts how IMNS as electronic skin elements could be used for various components of closed loop bidirectional neural prosthesis.

In block 1, a large area printed IMNS based flexible FET array is envisaged to be used as an addressable readout interface to address the tactile sensors of the electronic skin. Further, the IMNS itself could form as a part of a static or dynamic sensor [41,220,218] as explained in the previous section. Some practical implementations of these are discussed in the subsequent chapters.

In block 2, a biomimetic tactile data processing strategy has been proposed based on a neural nanowire FET (ν-NWFET) device as a building block. This is in order to mimic the local data processing in the early sensory pathways of the tactile sensing nervous system. Further, details of this are presented in Chapter 9.

In block 3, there are two key components; (1) reading the neural signals and interpreting them reliably to decode the prosthesis user's intention, and (2) writing to the neurons to give feedback to the user. Nanowire FETs find application in reading from the neurons [221,222], thanks to the higher sensitivity offered by the surface-to-volume ratio as well as for decoding the neural signals such as spike sorting. Currently, there is no stable, long lasting, reliable solution for writing to the neurons. A promising solution is an optogenetic neural interface which uses genetically modified microbial opsins, or light-sensitive ion channels that are specific to nerves, for control of neural signalling [23]. The nerves can be excited or inhibited

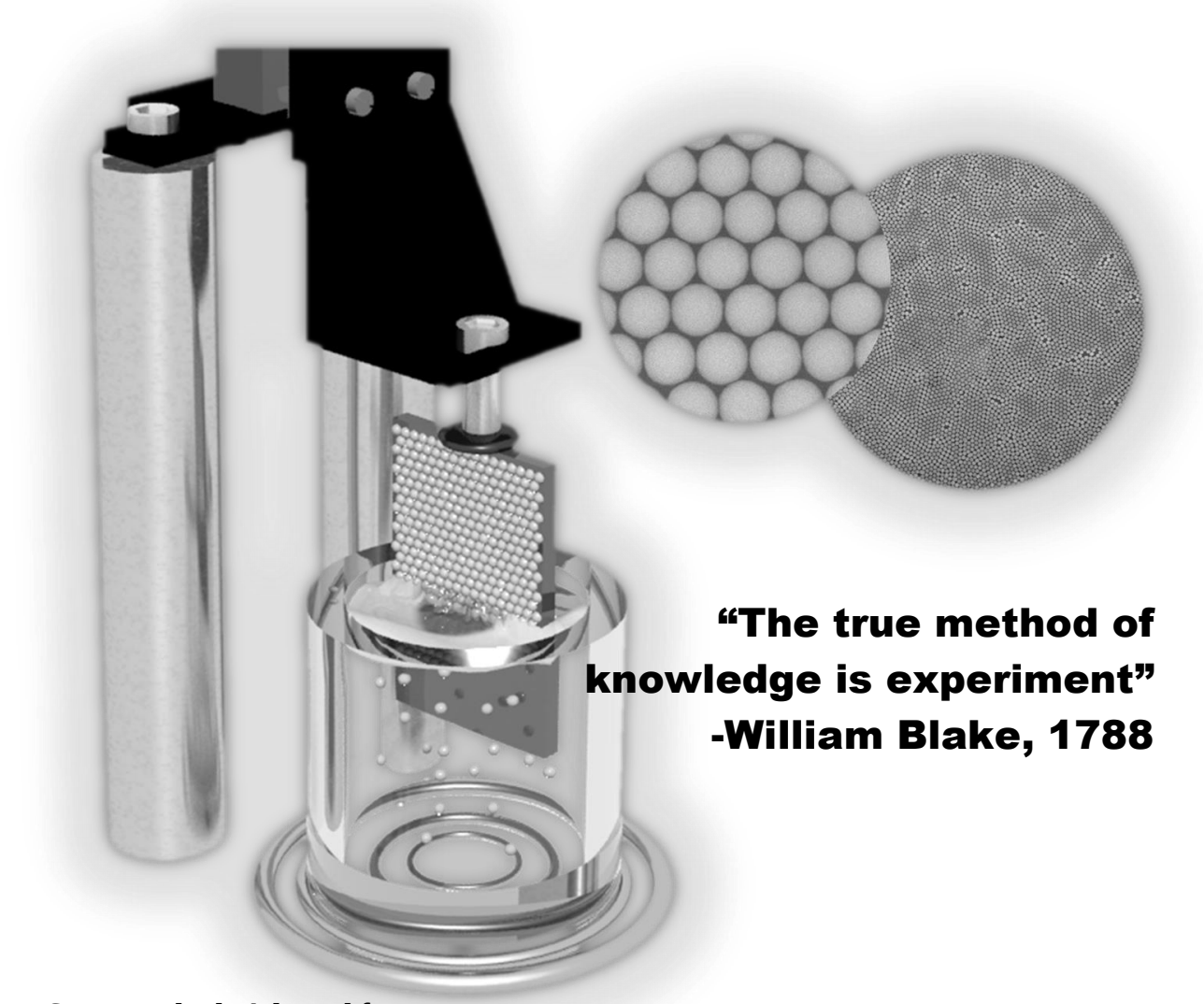
by specific wavelengths of light. Signal control at the biochemical level can be achieved with optogenetics interface without physical contact between the nerve and the electrode. Towards optogenetic neural interface, ultra-thin silicon membrane based JLFETs or equally UTCs could be used as μLED drivers.

2. 5. Summary

Overall, the focus of my research has been on exploring novel strategies for electronic circuits and system development based on flexible IMNS as a building block. The major application targeted is tactile e-skin for prosthesis and robotics. The developed technology acts as a platform for realizing many futuristic applications. IMNSs are one of the best building blocks for fabricating a wide range of sensors, high-performance devices and systems. The next chapter presents the methods and tools used for this research and subsequent chapters present the work done towards the practical realisation.

3

Methods



“The true method of knowledge is experiment”
-William Blake, 1788

Some Methods Adapted from

C. G. Nuńez[#], W. T. Navaraj[#], F. Liu, D. Shakthivel, R. Dahiya, "Large-Area Self-Assembly of Silica Microspheres/Nanospheres by Temperature-Assisted Dip-Coating", ACS Appl. Mater. Interfaces 2018, 10, 3058−3068, [#]Equal Contribution.

Contents

3. Methods

This chapter presents details on the experimental (fabrication and characterisation) tools employed to carry out the outlined research work. The devices and structures presented in this thesis were fabricated and characterised using the various equipment available at the University of Glasgow, mainly in the James Watt Nanofabrication Centre (JWNC), the Bendable Electronics and Sensing Technology (BEST) group laboratory and the Electronics System Design Centre (ESDC). The detailed fabrication procedures of various devices/structures are outlined in the subsequent chapters, while an overview of the key techniques is provided in this chapter.

The experimental tools include metallisation tools (namely electron beam evaporation, thermal evaporation, sputtering), dielectric deposition systems (namely plasma enhanced chemical vapour deposition (PECVD), Inductively Coupled Plasma Chemical Vapour Deposition (ICP-CVD), Atomic Layer Deposition (ALD)), lithography tools (photolithography, electron beam lithography), characterisation tools (such as semiconductor parameter analyser, optical and electron microscopes) etc. Custom developed tools/setup are also explained in this chapter, namely temperature-assisted dip coating setup, contact printing setup and large-area DEP setup. The simulation/modelling tools include Silvaco TCAD, Matlab, Multisim and SimBrain.

3. 1. Micro/nano-fabrication tools and techniques

3.1.1. Lithography

Lithography (Greek: Lithos-stone, Graphein-writing) is a process used to realise patterns on a material (commonly known as ‘resist’). The patterns on resist are subsequently used as a mask to allow for the selective processing of underlying material[223]. The primary lithographic technique employed to realise various devices and structures in this thesis is photolithography while e-beam lithography has been used to make test patterns for nanowire synthesis as well as for fabricating ν-NWFET presented in chapter 8 of this thesis. There are various lithography techniques, such as optical lithography, electron-beam lithography (EBL), nanoimprint lithography, multiphoton lithography, scanning probe lithography and nanosphere lithography. When exposed to radiation, the resist goes through a chemical change which results either in the break-down of the molecular chains making it more soluble in developer (positive photoresist), or in it undergoing crosslinking between the molecular chain making it less soluble (negative photoresist) as illustrated in Fig. 3-1.

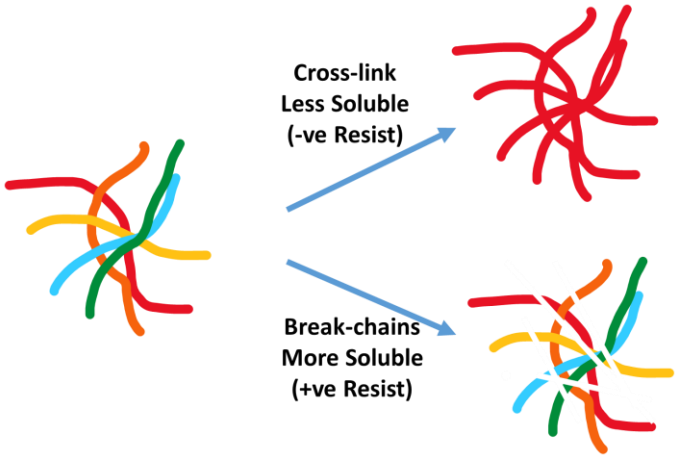


Fig. 3-1: Illustration of crosslinking or breaking up of polymer chains of resist after exposure to radiation.

Parameters such as resolution, registration or alignment accuracy between layers, throughput, associated cost, and resist compatibility for further processing are typically considered while determining the most appropriate lithography method. After lithography, further processing is carried out such as dry or wet etching (to remove material selectively) or metallisation followed by lift-off of metal from unintended regions.

3.1.1.1. Photolithography

As the name implies, photolithography uses light (typically in ultraviolet (UV) wavelengths) to create patterns on a photoresist. Fig. 3-2 illustrates the resist profiles for both positive and negative resists after photolithographic exposure followed by development. The wavelength of the light is a limiting factor in deciding the resolution of photolithography [224].

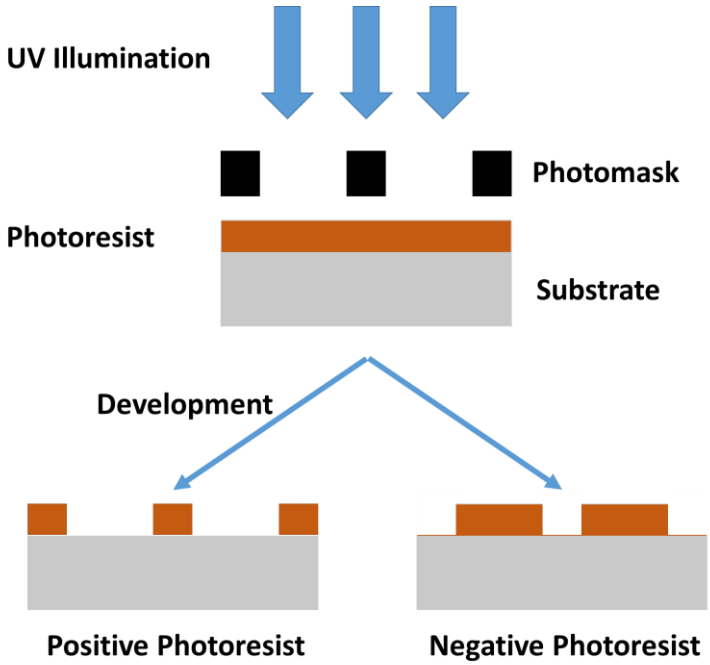
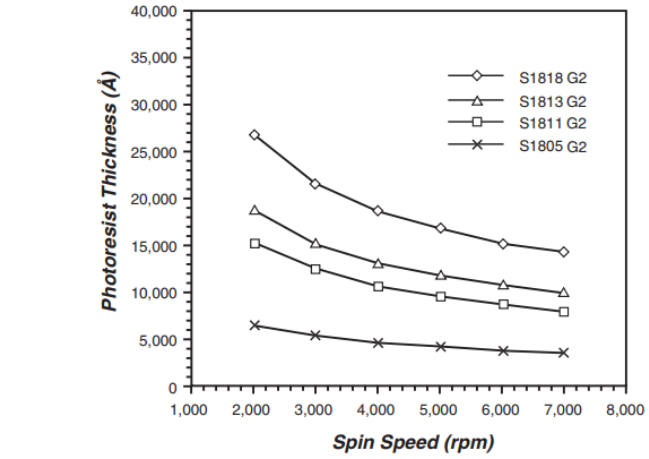


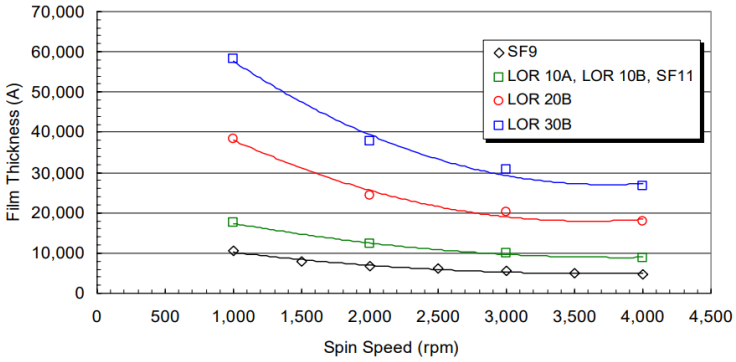
Fig. 3-2: Illustration of photolithography followed by development.

Other than nanoscale definition, photolithography was widely used for realising the device or structural patterns presented in this thesis. The work presented in this thesis was carried out using a Suss Microtec Mask Aligner 6 (MA6) with a 350 W mercury lamp. S1800 series photoresists were used for lithography and were spin-coated with a controlled spinner system with a vacuum chuck. Mainly, S1805 (which provides a thickness of ~0.5 µm when spun at 4000 RPM) and S1818 (which provides a thickness of ~1.8 µm when spun at 4000 RPM) photoresists were used with hexamethyldisilazane (HMDS) as an adhesion promotor on dehydrated substrates. The spin speed vs thicknesses of various S1800 and LOR series resists are shown in Fig. 3-3(a) and (b), respectively. The photomasks were designed in the Tanner L-Edit tool and were fabricated using EBL. The photomask has transparent (quartz or glass) and opaque (to UV) regions (chrome or ferric oxide on quartz or glass) such that UV light can pass through the transparent regions and expose the photoresist on the substrate. The substrate and the photomask with the desired pattern to be transferred were loaded in to the mask aligner. The photomask and the substrate were brought into contact and the photoresist was exposed using the UV illumination from the mercury source, thereby transferring the pattern engraved on the photomask into the photoresist. For multi-level

lithography, alignment markers were used to align the photomask to the patterns on the substrate before UV exposure.



a



b

Fig. 3-3: Spin speed vs thickness for various (a) S1800 series photoresists and (b) LOR resists[226,227].

The typical recipes used for photolithography processes are described below:

Photoresist S1805:

S1805 was primarily used where a pattern with a minimum resolution of ~5 µm or less was required.

1) The sample was cleaned and blow dried with N_2 gas.
2) The sample was then given a dehydration bake at 120˚C in a convection oven for 30 minutes.
3) The sample was placed on the vacuum chuck of the spinner system and vacuum was enabled.
4) HMDS was drop casted and spun on to the sample at 4000 RPM speed for 30 seconds.
5) S1805 photoresist was filtered through a Poly Tetra Fluoro Ethylene (PTFE) syringe filter and spun on to the sample at 4000 RPM for 30 seconds.
6) The sample was pre-baked at 115˚C for 60 seconds on top of a hot plate.
7) The sample and the photomask were loaded in MA6, aligned (if required) and exposure was carried out in hard contact mode with CH1 for 2.3 seconds.
8) The sample was developed in MF319 developer for 75 seconds.
9) The sample was rinsed in running RO water for 3 minutes and then blow dried with N_2 gas.

10) The sample was observed through an optical microscope and if required post-baking at 120˚C for 35 minutes in a convection oven was carried out.

Photoresist S1818:

S1818 was primarily used where a pattern with a minimum resolution of >5 µm was required.

1) The sample was cleaned and blow-dried with N_2 gas.
2) The sample was then given a dehydration bake at 120˚C in a convection oven for 30 minutes.
3) The sample was placed on the vacuum chuck of the spinner system and the vacuum was enabled.
4) HMDS was drop casted and spun on to the sample at 4000 RPM speed for 30 seconds.
5) S1818 photoresist was filtered through a Poly Tetra Fluoro Ethylene (PTFE) syringe filter and spun on to the sample at 4000 RPM for 30 seconds.
6) The sample was pre-baked at 115˚C for 180 seconds on top of a hot plate.
7) The sample and the photomask were loaded in MA6 and exposure was carried out in hard contact mode with CH1 for 6 seconds.
8) The sample was developed in MF319 developer for 2 minutes and 30 seconds.
9) The sample was rinsed in running RO water for 3 minutes and then blow dried with N_2 gas.
10) The sample was then observed through an optical microscope and if required post-baking at 120˚C for 35 minutes in a convection oven was carried out.

Bi-layer Metal Lift-off with S1818 and LOR10A:

Patterned metallisation was carried out using bi-layer metal lift-off for the devices/structures presented in this thesis. Wherever metal lift-off was required, the following recipe was used which involved LOR10A resist as the bottom layer with S1818 as the top layer. LOR stands for lift-off-resist which acts as a sacrificial undercut layer in bilayer lift-off processing as illustrated in Fig. 3-4.

1) The sample was cleaned and blow-dried with N_2 gas.
2) The sample was then given a dehydration bake at 120˚C in a convection oven for 30 minutes.
3) The sample was placed on the vacuum chuck of the spinner system and the vacuum was enabled.
4) LOR10A was drop casted and spun on to the sample at 6000 RPM speed for 30 seconds.
5) The sample was pre-baked at 160˚C for 120 seconds on top of a hot plate.
6) S1818 photoresist was filtered through a Poly Tetra Fluoro Ethylene (PTFE) syringe filter and spun on to the sample at 4000 RPM for 30 seconds.
7) The sample was baked at 115˚C for 180 seconds on top of a hot plate.
8) The sample and the photomask were loaded in MA6 and exposure was carried out in hard contact mode with CH1 for 6 seconds.
9) The sample was developed in MF319 developer for 2 minutes and 30 seconds. During this developing the LOR resist forms an undercut as illustrated in Fig. 3-4.
10) The sample was rinsed in running RO water for 3 minutes and then blow dried with N_2 gas.

11) The sample was then observed through an optical microscope.
12) The sample was treated in plasma asher at 90 W for 2 minutes just before the metallisation.
13) The desired metal stack was deposited on the top of the patterned bilayer resist using one of the metallisation techniques presented in the next section.
14) This was followed by lift-off of the undesired metal on top of the resist stack by stripping the resist in 1165 stripper. The sample was then squirted/rinsed with Iso-propyl Alcohol (IPA) followed by RO water.

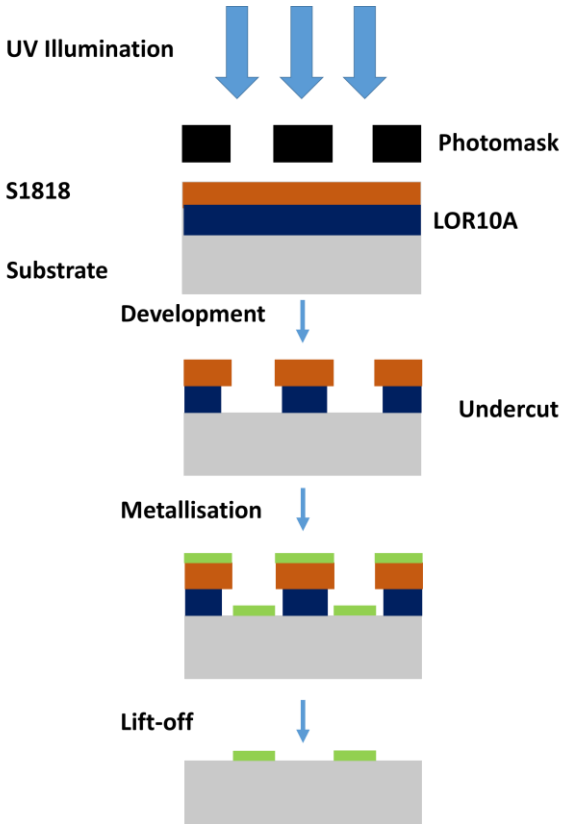


Fig. 3-4: Schematic illustration of bi-layer metal lift-off process.

3.1.1.2. Electron Beam Lithography (EBL)

The critical nanopatterning was carried out using Vistec VB6 EBL tool with Poly(methyl methacrylate) (PMMA) as resist. In contrast to photolithography where a pattern gets transferred from the photomask to the resist all at once, the EBL uses a direct write method. A beam of electrons is focused on to an electron-sensitive resist layer on the specific area to be radiated so as to draw the required shapes and patterns. The e-beam undergoes a raster or a vector scan with beam blanking wherever the radiation is not required. In case of raster scanning, the beam scans over the whole sample surface, with the beam getting blanked off in the region where the pattern is not required. In the case of vector scanning, the beam only scans over the region where the resist is to be exposed because of which vector scanning is faster than the raster method. [3]. The Vistec VB6 uses the vector scanning method. While this process does not require any photomask and offers increased flexibility, the process is slower because of the inherent serial nature and expensive compared to photolithography. Fig. 3-5 shows the typical process flow followed for the nanopatterning of various structures during this thesis . The process starts with the design of the structures and patterns in the Tanner L-Edit CAD tool. The design file is then exported in the GDSII file format. The GDSII file is fractured using Beamer software from which it is transferred to the VB6 EBL

tool. The pattern is fractured in smaller sub-parts, each referred to as main fields. Main fields are navigated by the mechanical movement of the stage in the EBL tool. Within the field, the patterning is carried out by the electromagnetic deflection of the coils. Stitching is carried out between the main field regions during EBL writing. Another software package called Belle is used through which various parameters are set namely,: substrate information, resolution, dose, beam spot size (BSS), variable resolution unit (VRU).

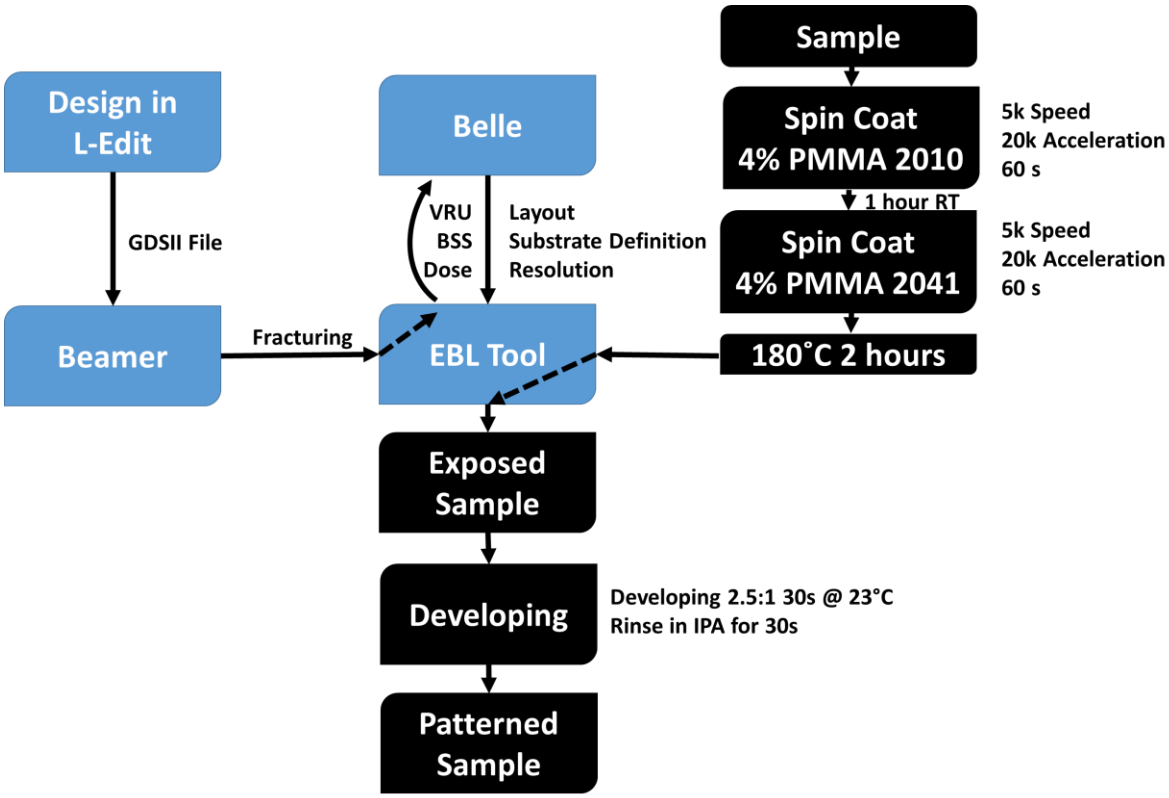


Fig. 3-5: Process flow followed for EBL

During EBL exposure, the tool exposes a point in the resist with the e-beam then steps to the next point and so on until that shape is completed. This stepping of beam (known as BSS) is illustrated in Fig. 3-6 and is related to the VRU as given by the equation :

BSS=Resolution x VRU (**E 3-1**)

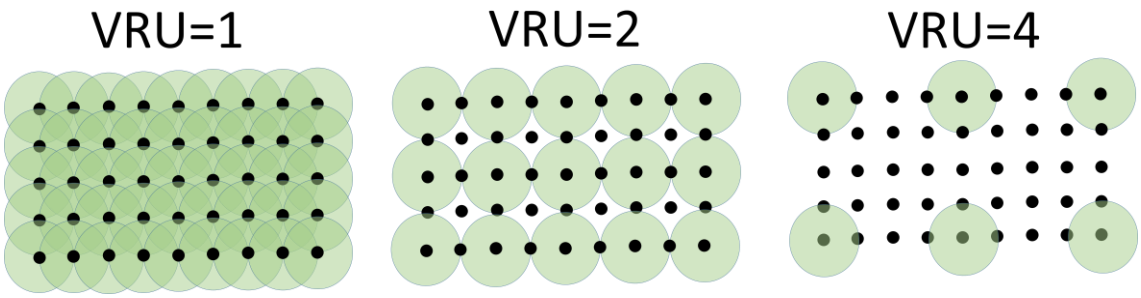


Fig. 3-6: Illustration of beam step size for variable resolution unit, VRU = 1, VRU = 2 and VRU=4.

The dots-on-the-fly technique was used for realising the dot-array pattern which was subsequently used to realise vertical nanowires. In this case as shown in Fig. 24, the dose was kept less than the clearing dose and the VRU was kept higher (eg. VRU=4 as shown in

Fig. 3-6) which results in dot patterning on the fly without drawing individual dots in the layout. Further details are presented in chapter 7 section 7.2.3 of this thesis.

3.1.2. Metallisation

Metallisation is important to realise contacts, gate(s), and interconnects for various IMNS devices as well as barrier and catalytic material for MACE NWs synthesis. Physical-vapour deposition (PVD) was the major technique through which metallisation was carried out for the devices/structures presented in this thesis. Primarily, two techniques were used: (1) Electron Beam Evaporation (EBE) and (2) Thermal Evaporation. Sputtering (with a table top plasma sputter tool) was occasionally used to coat samples with Au metal in order to improve conductive coverage and contrast for scanning electron microscopy (SEM) by eliminating the charging of insulating samples.

3.1.2.1. Electron Beam Evaporation (EBE)

EBE was mainly carried out by using the Plassys MEB 550S and MEB 400S systems. Both systems are almost similar except that MEB 550S has an ion gun for substrate cleaning and etching and can handle samples with up to a 150 mm diameter, whereas 400S can process up to 100 mm. Both systems have a 10 kW electron beam source, planetary motion capability, cryo pumps with load lock capability, and *in situ* crystal thickness monitor with full computer control. MEB 550S also has the capability for angled evaporation.

EBE is normally carried out in a vacuum ($<10^{-7}$ mBar) during which an electron beam (typically generated by thermionic emission from a tungsten filament) is used to melt a metal target which eventually undergoes evaporation. The evaporated metal reaches the sample and deposits to form a film of required thickness. The various metals used for the different devices/structures reported in this thesis include aluminium, titanium, gold, platinum (only MEB 400S) and nichrome.

3.1.2.1. Thermal Evaporation

A thermal evaporator system employing tungsten filament-based resistive joule heating was used to deposit silver for the MACE Si NWs synthesis process. The system has a glass bell jar with diffusion pump for pumping down the jar to low vacuum before evaporating Ag metal. 6 thermal sources (with the choice of tungsten and/or ceramic boats and a wide choice of metal sources such as Ag, Au, Ni) can be loaded at a given time with a switching unit for choosing a particular thermal source. A current transformer was used to control the current which controls the evaporation rate. The deposition rate and thickness were monitored by a crystal thickness monitor *in situ*.

3.1.3. Dielectric Deposition/growth

Various functional and sacrificial dielectric layers used in the fabrication of the devices/structures of this thesis were realised mainly from four techniques: (1) Plasma Enhanced Chemical Vapour Deposition (PECVD) (2) Inductively Coupled Plasma Chemical Vapour Deposition (ICP-CVD), (3) Atomic Layer Deposition (ALD) and (4) Thermal Oxidation.

3.1.3.1. Plasma Enhanced Chemical Vapour Deposition (PECVD)

Typically, a PECVD system comprises two parallel plate electrodes within a vacuum chamber where the sample to be coated is placed over one of the electrodes[223]. The system

normally has a substrate heating arrangement. Compared to an Atmospheric Pressure CVD (APCVD) or Low Pressure (LPCVD), PECVD can be used to deposit films at relatively lower substrate temperature, thanks to the reactive plasma. This enables the deposition of dielectric thin films on flexible materials which otherwise cannot be subjected to the high temperatures of APCVD or LPCVD. Reactive gases are fed into the reaction chamber and controlled by mass flow controllers and a throttle valve which maintains the vacuum conditions. A radio frequency (RF) voltage is applied between the electrodes, resulting in the formation of a plasma between the electrodes. The plasma activates the reactive gases resulting in the growth of the dielectric film on the substrate. An oxford Instruments PECVD 80+ system was used in this research mainly to deposit SiO_x film for various devices/structures while thermal oxidation was used to achieve high quality stochiometric SiO_2 for gate dielectric material.

Table 6: Recipe used for SiO_x deposition

Material	Recipe
SiO_x	Tool: PECVD 80+ SiH_4: 7 sccm N_2O: 200 sccm N_2: 85 sccm RF Power: 15 W Pressure: 1000 mTorr Temperature: 300°C

3.1.3.2. Inductively Coupled Plasma Chemical Vapour Deposition (ICP-CVD)

The principle of electromagnetic induction is used in ICP-CVD to create a high-density plasma that allows for the deposition of dielectric materials at lower temperatures than PECVD and with improved material quality[228,229]. In this thesis, the Oxford Instruments System 100 ICP 180 PECVD was used for depositing silicon nitride.

Table 7: Recipe used for SiN_x deposition using ICP-CVD

Material	Recipe
SiN_x	Tool: ICP180 SiH_4: 7.2 sccm N_2: 6 sccm RF Power: 100 W Pressure: 4.4 mTorr Temperature: 35°C

3.1.3.3. Atomic Layer Deposition (ALD)

Atomic Layer Deposition is a technique that enables the deposition of thin film materials of metals and metal oxides with excellent control over the thickness and, layer-to-layer composition with highest conformality out of the various deposition techniques. Most ALD processes are carried out at moderate temperatures (<350˚C). This makes it suitable for depositing on flexible substrates. In ALD, chemical precursors in gaseous form are pulsated alternately in cycles through a vacuum chamber (<1 Torr) with optional purge stages in between. The reactions (referred to as half-reaction) are self-limiting, forming a self-assembled monolayer (SAM) on the surface of the substrate. The reaction can take place

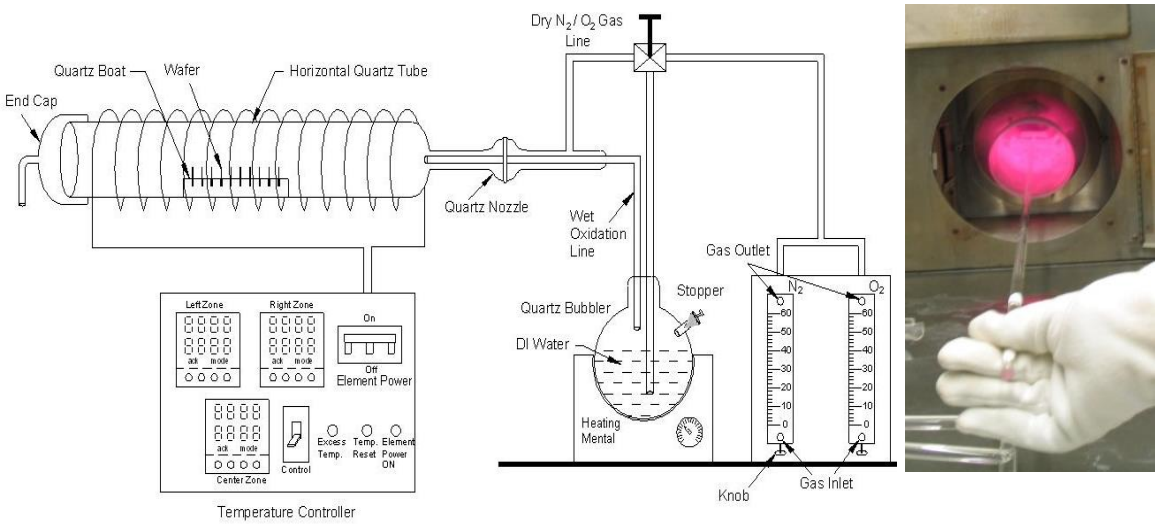
even in deep trenches and hence the conformality is achieved. Then the chamber is purged by an inert gas to remove the unreacted precursors. This is followed by a pulsation of the next precursor cycle and so on. Sequential pulsation of all the precursors through the chamber is called a cycle. The typical thickness after each cycle is in the order of the angstrom scale. The total number of cycles determines the final thickness and thus offers an excellent control of the thickness. Different temperature ranges are suitable for various ALD processes, called ALD temperature windows.

During this thesis, the ALD technique was mainly used for depositing Al_2O_3 as gate dielectric for various devices. The depositions were carried out using the Oxford Instruments FlexAL system which has the capability for both plasma as well as thermal ALD. The system has a capacity to handle up to 200 mm diameter substrate with load lock facility, a plasma source and a heated stage with a capability of up to 400˚C. The tool is capable of depositing various materials including Al_2O_3, HfO_2, ZrO_2, TiN, TaN, WN, AlN and Pt.

3.1.3.4. Thermal Oxidation and Diffusion Furnace

A horizontal thermal furnace was used for the oxidation and doping of wafers through thermal diffusion. The furnace which was used for thermal diffusion and oxidation comprised of

- a cabinet
- a heating assembly
- a fused quartz horizontal process tubes where the wafers undergo oxidation or diffusion
- a digital temperature controller and measurement system
- a system to monitor and control the flow of gases into and out of the process tubes and a loading station used for loading (or unloading) wafers into (or out of) the process tubes as shown in Fig. 3-7.



a b

Fig. 3-7: (a) Schematic diagram [223] and (b) photograph of horizontal thermal oxidation/diffusion furnace

The heating assembly consists of several heating coils that control the temperature around the quartz tube. Mass flow controllers are used to control the flow rate of gases. In addition to this a solid boron source or a phosphorus source is used for carrying out the doping of semiconductor wafers.

3.1.4. Etching

Etching is an important subtractive technique used in micro/nano-fabrication to achieve desired structures. Based on the chemicals and the by-products of etching process, it could be termed as wet or dry etching. Depending upon the profile or features achievable through etching it could be termed as isotropic or anisotropic etching as illustrated in Fig. 3-8.

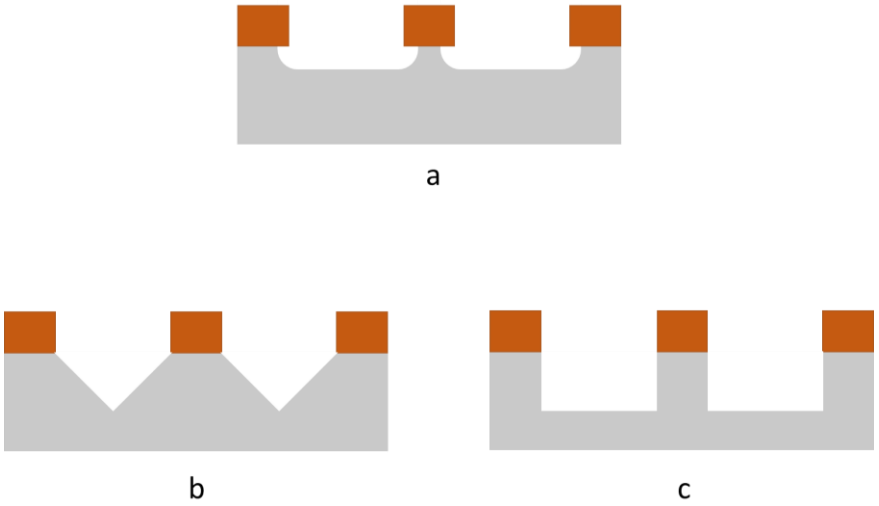


Fig. 3-8: Schematic diagrams of the etch features (a) isotropic (b, c) anisotropic etching

3.1.4.1. Wet Etching

Wet etching is normally carried out by removing material through chemicals in liquid state. The chemicals were chosen to target a specific material and to achieve a desired etch rate. During this doctoral research, wet etching was used for etching silicon, silicon oxide, silicon nitrides and aluminium oxide. Sometimes, the dielectric films were etched using dry etching as mentioned in the respective process procedures.

Wet etching was extensively used in this research work. Buffered Oxide Etchant (BOE), a mixture of 49% HF:40% NH_4F (1:5) in H_2O was used for etching silicon oxide which gives a etch rate of ~100 nm/minute. A slower rate of SiO_x etching was achieved by using dilute HF acid (1:50 49% HF:H_2O). In the fabrication of UTCs, 25% TMAH in H_2O and 10% IPA was used to thin down the silicon. In the fabrication of NR-JLFET, wet etching was used for etching silicon etch and SiO_x etch. Ultra-thin silicon ribbon was realised by wet etching in a solution of nitric acid (HNO_3), water (H_2O) and ammonium fluoride (NH_4F) in the volume ratio of 126:60:5 (HNO_3: H_2O: NH_4F). MACE was carried out in HF:H_2O_2:H_2O in various ratios depending on the catalytic material and other requirements as explained in chapter 7.

3.1.4.1. Dry Etching

Etching processes in which the etchants and byproducts are in gaseous form are referred to as dry etching. Dry etching can result in both an isotropic profile as well as anisotropic profile. Dry etching where chemical reactions are the major etching mechanism generally result in an isotropic profile whereas instances where a physical process such as bombarding ions causes etching results in anisotropic profile. The former generally has a higher selectivity while the latter has higher directionality. A combination of physical and chemical etching occurs in the case of reactive ion etching (RIE) thereby the etching profile can be tuned and controlled. In the case of RIE (illustrated in Fig. 3-9), a high-power RF input is applied between two electrodes in the reaction chamber forming a plasma of the reactive gases. The radicals in the plasma are highly reactive. They undergo chemical reaction with the molecules in the surface of the sample and thus make the etch selective; whereas the ions gain high kinetic energy and are accelerated towards the grounded electrode where the sample is placed. The energetic ions bombard the surface causing an anisotropic etching profile.

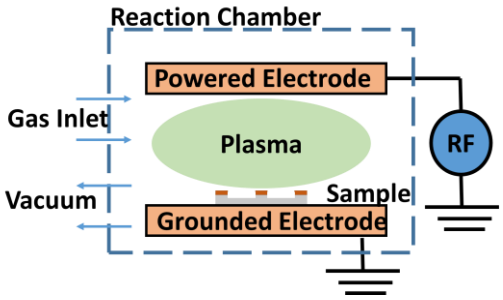


Fig. 3-9: Schematic illustration of RIE system

The Oxford Instruments RIE80+ tool was the major RIE equipment used in this research for etching silicon nitride and silicon oxide with trifluoromethane/oxygen (CHF_3/O_2) and trifluoromethane/argon (CHF_3/Ar) as etching gases, respectively.

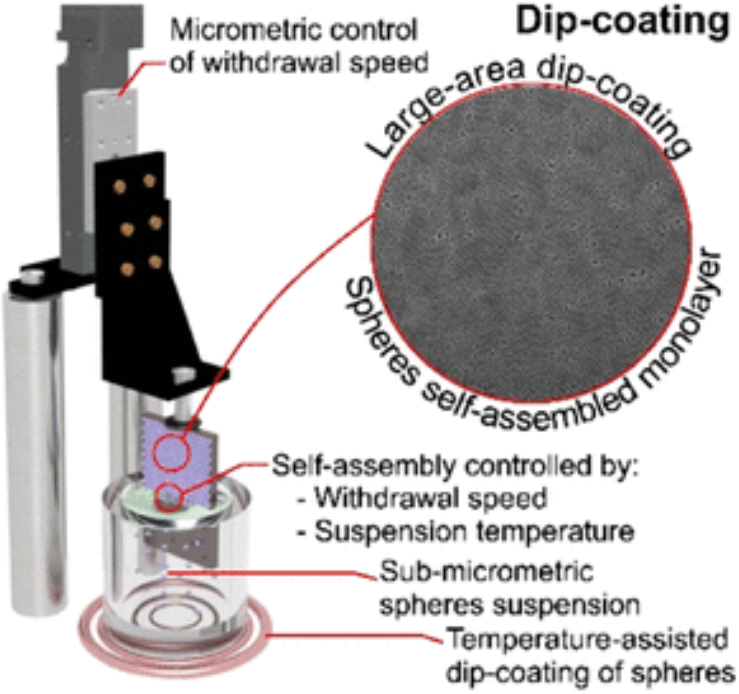
Table 8: Recipe used for RIE

Material	Recipe
Al_2O_3	Tool: RIE 80+ Argon plasma CHF_3: 25 sccm Ar: 18 sccm RF Power: 200 W Pressure: 30 mTorr Temperature 20˚C Etch Rate: 4 nm/minute
SiO_2	Same as Al_2O_3 recipe Etch Rate: 39 nm/minute
PECVD SiN_x	Tool: RIE 80+ CHF_3: 50 sccm O_2: 5 sccm RF Power: 150 W Pressure: 55 mTorr Temperature: 20 °C Etch Rate: 50 nm/minute

3.1.4.2. Ashing of Organic Residue

Polymer resist and other organic residues in the samples were removed by using oxygen (O_2) plasma ashing in a Plasmaprep 5 Barrel Asher.

3.1.5. Temperature-assisted Dip-coating System



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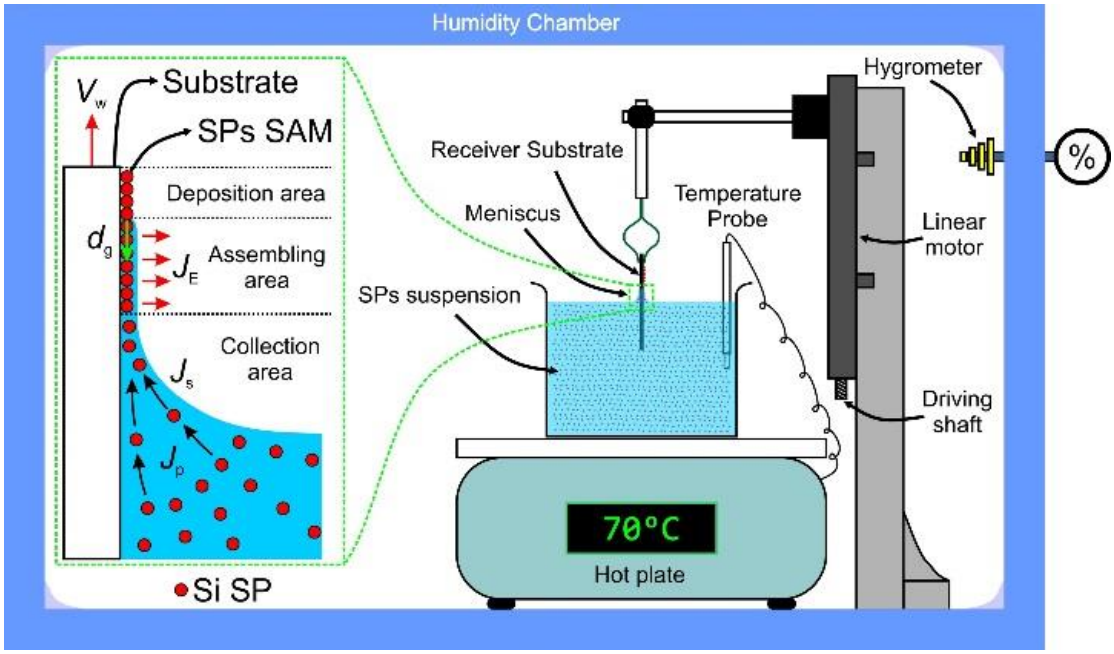


b

Fig. 3-10: (a) 3D and (b) 2D schematic illustration of dip-coating setup for large area assembly of silica spheres. Inset: self-assembly process of SiO_2 SPs driven by dip-coating [27] Carried out in collaboration with CGN, FL, DS, RD. Reprinted (adapted) with permission from ACS Appl. Mater. Interfaces, 10 (3), 2018. Copyright 2018 American Chemical Society.

As presented in section 2.3.3.3 and illustrated in Fig. 2-10, MACE is one of the promising routes for fabricating semiconductor nanowires with a controlled diameter, length, density, structure, orientation and doping [172] each of which are prerequisite to realise high-performance flexible electronics. In order to get nanowires of controlled density and diameter, the initial nano-mesh has to be patterned. In order to achieve this, one of the simpler low-cost method is to use nano-sphere colloidal assembly-based patterning, also known as Nanosphere Lithography (NSL) followed by the MACE process; the details are given in chapter 7 (refer to Fig. 7-12). A temperature-assisted dip-coating process has been used to assemble silica micro/nanospheres (SPs) on silicon substrates over large areas. The SAM of these spheres were used to carry out NSL to create metal nano-mesh patterns which were subsequently used for synthesising nanowires using the MACE process. The detailed results of MACE are presented in chapter 7 section 7.2.3. Here, the large-area temperature-assisted dip-coating setup is explained in detail.

Dip-coating is a simple cost-effective process for large scale coating. Surprisingly, this technique has not been extensively explored for large-area coatings of micron and sub-micron particles. The advantages of the work reported here, with respect to conventional dip-coating procedures, include larger micro/nanospheres SAM surface coverages and better control over the SPs SAM stripe-pattern morphology by using the temperature-assisted dip-coating approach (see Table 1 of [27]). The mechanism governing the dip-coating process is known as convective assembly[230] and has features similar to those observed in three-dimensional (3D) colloidal crystals obtained in particle assembly in slits between solid plates.[231] In the dip-coating method, SPs are assembled on the substrate surface by dipping the substrate in the colloidal suspension and slowly withdrawing the substrate from the suspension, or keeping the substrate position and evaporating the solvent.[232]

Fig. 3-10 shows the 3D and 2D schematic illustration of the custom-made setup built for the dip-coating process. The set-up permits control over different operational parameters, including receiver substrate withdrawal speed (V_w), withdrawal step length (L_w), withdrawal angle (θ_w) and temperature of the SPs suspension (T_s). Briefly, the withdrawal parameters determine the pulling conditions of the receiver substrate, with: i) V_w measured in μm/s setting the pulling speed of the receiver substrate from the SPs solution; ii) L_w measured in length units determining the stroke of pulling step which can cover lengths above or below sample lengths for uniform coatings of receiver substrate (discussed in sections 7.2.4.4.1 and 7.2.4.4.2 of Chapter 7), and for strip-pattern based coatings (discussed in section 7.2.4.4.3 of Chapter 7), iii) θ_w measured in degrees setting the pulling angle of receiver substrate with respect to pulling direction (discussed in section 7.2.4.4.3 of Chapter 7). The whole setup has been placed inside a custom-made humidity chamber, consisting of a cube of acrylic glass with a silicone seal at the edges, to enhance the reproducibility of the process by preventing air convection effects. Both, the temperature and RH of the environment have been measured *in-situ* using a digital hygrometer (HTD-625). The top side of the chamber was modified by creating a distribution of holes to reduce the relative humidity (RH) of the chamber down to constant values of around 20%. The use of a low RH allows the evaporation of solvent from SPs solution at rates in the range of 0.1-10 μm/s, which is approximately in the range of speeds that will be used to withdraw the receiver substrate. In addition, the humidity chamber has been placed on top of an optical table (from Newport) to prevent any external vibration during the dip-coating experiments.

Prior to the dip-coating process, the SPs suspension is sonicated for 5 minutes and heated up to temperatures ranging between 25°C (room temperature, RT) and 80°C. The suspension

is heated by using a hot plate (Stuart, CD162) with a polytetrafluoroethylene (PTFE)-coated temperature probe for good control over T_s. Then, a hydroxylated Si substrate is vertically attached to a 3D printed platform – forming a θ_w of 0^o – which is driven by a linear motor (VT-21 Linear Stage from Micronix USA) and controlled by LabVIEW. Initially, the sample is slowly dipped in the pre-heated suspension at a speed of 5 µm/s and kept in that position for 2 min (immersion time, t_i) then, the sample is pulled out the SPs suspension at a controlled V_w until the entire sample area is outside the SPs suspension. The effect of various parameters on the performance of the system is discussed in section 7.2.3 of chapter 7.

3.1.6. Printing of Nanowires

The previous section described a nano-patterning strategy for synthesising Si nanowires. As shown in Fig. 7-1, after synthesis, the vertical nanowires have to be printed on flexible substrates for realising high-performance flexible electronics. Two approaches were used for printing:

1) Large-area DEP assisted printing (presented in section 7.3.3 of chapter 7)
2) Contact printing (setup presented here while key results are presented in section 7.3.1 of chapter 7)

3.1.6.1. Contact printing setup

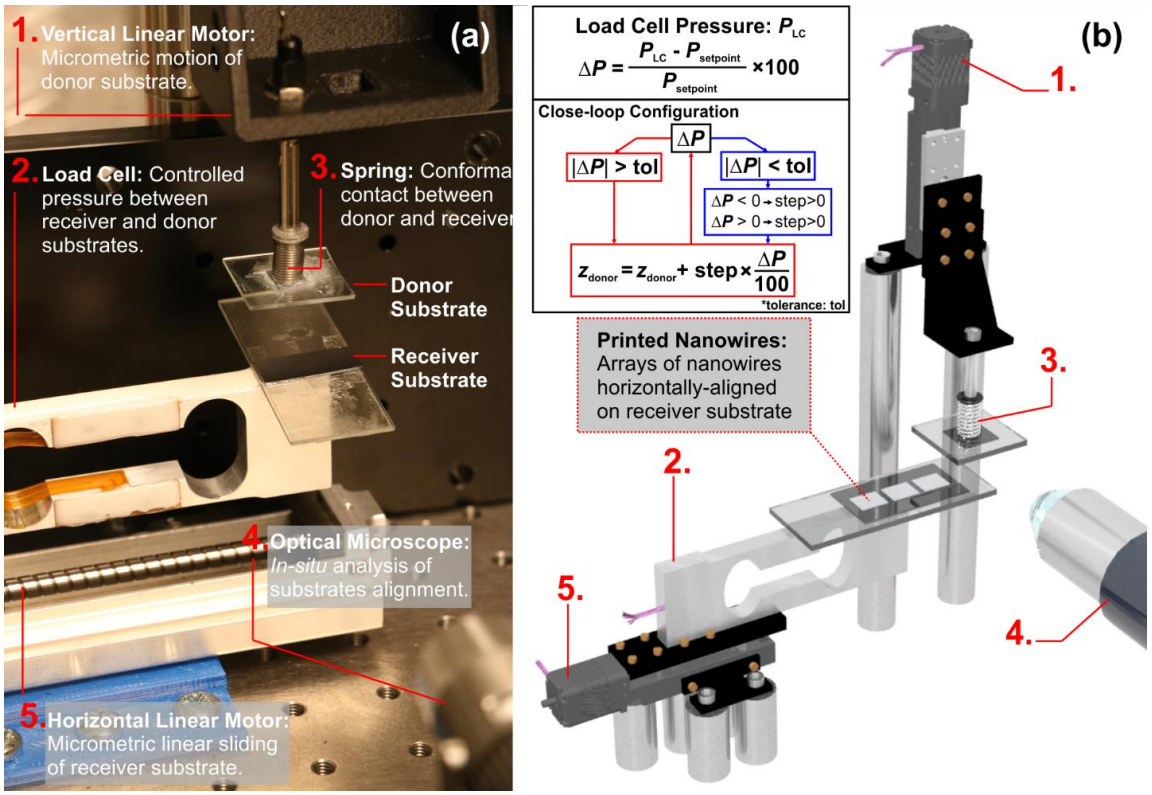


Fig. 3-11: Description of contact-printing setup (a) photograph and (b) schematic illustration of the contact-printing system. [233]Carried out in collaboration with CGN, FL, DS. Nature: Microsystems & Nanoengineering, 4, 22 (2018) CC BY 2.0.

The indigenously developed contact-printing system used for printing nanowires is presented in Fig. 3-11, published in [29], including a photographic picture (Fig. 3-11(a)) and 3D schematic illustration (Fig. 3-11(b)). The system consists of: 1) a vertical linear position stage (VT-21 from Micronix USA) to control the position of the donor substrate; 2) a load cell (Model 1004 from Vishay) to measure the force exerted by the donor substrate when

coming into contact with the receiver substrate; 3) a three-dimensional (3D) printed platform with a spring to ensure the conformal contact between donor and receiver substrate; 4) an optical microscope (Digital Microscope 1.3M from RS Components) to analyse the alignment and conformal contact formed between donor and receiver substrates; and 5) a horizontal linear position stage (from Motorlink) to control the sliding of the receiver substrate during the contact-printing process. A linear stage motor allows for micrometric movement control of the donor substrate's vertical position with respect to the receiver substrate (1). The force exerted by the donor substrate on the receiver substrate is measured by a load cell placed underneath the receiver substrate (2). The spring attached to the donor substrate ensures its conformal contact with the receiver substrate (3), and the alignment is checked by *in-situ* analysis with an optical microscope (4). The system also allows controlling the sliding speed of the contact-printing by using a second linear stage motor (5). Inset: contact-printing experiments are carried out at a specific pressure controlled by a close-loop configuration described in the logic diagram. The load cell has a rated output of 0.9 mV/V, a maximum rated capacity of 6 N and a maximum excitation voltage of 10 V, which means that, the voltage-to-force conversion factor (exciting the load cell at 10 V) is around 0.67 N/mV. Accordingly, the contact force (F) exerted on the receiver substrate is measured as a function of the donor vertical displacement (z), resulting in a linear tendency given by F(N) = 0.55 + 8.7 z(mm) (Figure S2(a) in [29]). In addition, the sensitivity (S) of the load cell has been determined as a function of the motor step size (Figure S2(b) in [29]), aiming to determine the minimum step size that can be used to produce a significant variation in the force measured by the load cell. From this study, it has been concluded that S of the load cell is around 5% for steps of 5 µm. Accordingly, contact-printing experiments carried out in this work use a minimum step size of 5 µm, allowing an accurate measurement over the applied force range.

Once the donor substrate area and the set-point pressure ($P_{\text{set-point}}$) are given to the software, the close-loop configuration of the system (Fig. 3-11(b)), with control parameters such as the approaching step size and the tolerance (tol), allows it to reach $P_{\text{set-point}}$ within a short period of time (< 1 min). A user-friendly Labview interface has been developed to guide the user at each step of the contact-printing process (see Fig. S3. in [29]). Firstly, parameters such as donor substrate surface, contact pressure, sliding speed/stroke, vertical motor step length, and tolerance are defined in the program. Thereafter both donor and receiver substrates are loaded in the system. The vertical motor moves the donor substrate towards the receiver substrate. Once the system detects the contact formed between substrates through the load cell, the pressure measured at each step of the vertical motor (P_{LC}) is compared to $P_{\text{set-point}}$. If $P_{\text{LC}} < P_{\text{set-point}}$, the vertical motor step direction is kept forward, i.e. step × ΔP/100 < 0 and therefore the donor substrate moves towards the receiver substrate, and the step length magnitude is reduced proportionally to the difference between pressures ($\Delta P = 100\ (P_{\text{LC}} - P_{\text{set-point}})/P_{\text{set-point}}$), i.e. step = step × ΔP (being ΔP < 0 implying forward direction). On the other hand, if $P_{\text{LC}} > P_{\text{set-point}}$, the vertical motor moves the donor substrate backwards, reducing the pressure between substrates proportionally to ΔP. This approaching step continues until the tolerance is reached, i.e. $|\Delta P| \leq$ tol. Then, the receiver substrate slides at a speed (v_{sliding}) and along a stroke (l_{sliding}) programmed in the horizontal motor. The latter will allow for the control of the surface covered by NWs on a circuit layout as will be demonstrated later. A video recording of the above process is provided in the Supplementary Movie 2 in [29].

3. 2. Characterisation Tools

3.2.1. Scanning Electron Microscope (SEM)

The resolution of an optical microscope depends upon the wavelength of the incident light used for imaging. The resolution of a microscope tool is given by the Rayleigh criterion:

$$R = \frac{0.61\lambda}{\mathrm{n}\sin\theta} \quad \textbf{(E 3-2)}$$

Where,

λ is the wavelength of the incident wave

n is the refractive index of the medium

θ is the angle of the aperture of incident light.

A higher resolution can be obtained by using electrons for imaging instead of an optical source as the wavelengths of electrons are far lower compared to an optical wavelength (300 to 700 nm). The wavelength of the incident electron beam is given by the de Broglie wavelength equation:

$$\lambda = \frac{h}{p} = \frac{h}{m_0 v} = \frac{\mathrm{h}}{\sqrt{2m_0 eU}} \quad \textbf{(E 3-3)}$$

Where,

h is the Planck's constant

p is the momentum of the incident wave

m_0 is the rest mass of an electron

v is the velocity of the electron

e is the charge of the electron

U is the potential difference

For the typical value of potential difference, it can be estimated that the resolutions of SEM can reach up to few nanometres[223]. In the SEM, an electron beam from an emitter is focused into a fine probe by electromagnetic lenses which are subsequently raster scanned by electromagnetic deflectors over a small rectangular area. Various signals (secondary electrons, back scattered electrons, internal currents, photon emission, etc.) are created as the electron beam interacts with the sample, all of which can be detected by appropriate detectors. With ancillary detectors, the instrument is capable of elemental analysis. The SEM used for imaging various structures in this thesis were the FEI NovaNanoSEM and Hitachi S-4700 depending upon availability. Both are field emission scanning electron microscopes (FESEM). The immersion mode with charge neutralisation feature available in the FEI NovaNanoSEM was suitable for imaging structures on flexible substrates.

Main use: High magnification imaging and composition (elemental) mapping

Destructive: No, some electron beam damage

Magnification range: 10X – 3,00,000X is the typical operating range

Beam energy range: 500eV to 50keV; typically, 1 – 30keV

Sample requirements: Minimal, occasionally must be coated with a conducting film; must be vacuum

Sample size: Less than 0.1mm, and up to 10cm

Lateral resolution: 1 – 50nm in secondary electron mode

Depth sampled: Varies from a few nm to a few μm depending upon the accelerating voltage and the mode of analysis

Bonding Information: No

Depth Profiling: Indirect

3.2.1. Transmission Electron Microscope (TEM)

TEM was used for analysing crystallinity in nanowires. TEM analysis of the NWs was carried out in FEI Tecnai T20 system. The TEM system consists of LaB6 emission filament with maximum operating voltage of 200kV. Initially, the NWs were dispersed in DI water followed by mild sonication process. Carbon coated Cu grids of 300 mesh size was used in this study. The well dispersed NWs were transferred over the Cu mesh and dried under IR lamp for 30 minutes to remove all the moisture content. The structural characterisation was carried out through bright field (BF) and high resolution TEM (HRTEM) imaging at 160 kV beam condition.

3.2.2. Atomic Force Microscope (AFM)

The AFM, is a member of the scanning probe microscopy family. It operates by scanning an atomically sharp tip attached to a microcantilever horizontally across a surface thereby recording the topographical map of the scanned surface as illustrated in Fig. 3-12. A Bruker Dimension Icon AFM has been used for imaging various structures in this thesis mainly nanopatterns used for synthesis of nanowires and the resulting nanowires. The imaging was mainly carried out in tapping mode. A motorised stage is used for larger movements to locate the region for imaging via the camera. Once the region for imaging is located raster scanning is carried out during which the cantilever is moved up to atomic precision by the piezoelectric actuator. The cantilever moves owing to the force that the sample imposes on it. This is precisely recorded by measuring the associated displacement of a laser beam incident on the cantilever tip. This data is used to form a high-resolution image of the three-dimensional shape (topography) of the sample surface.

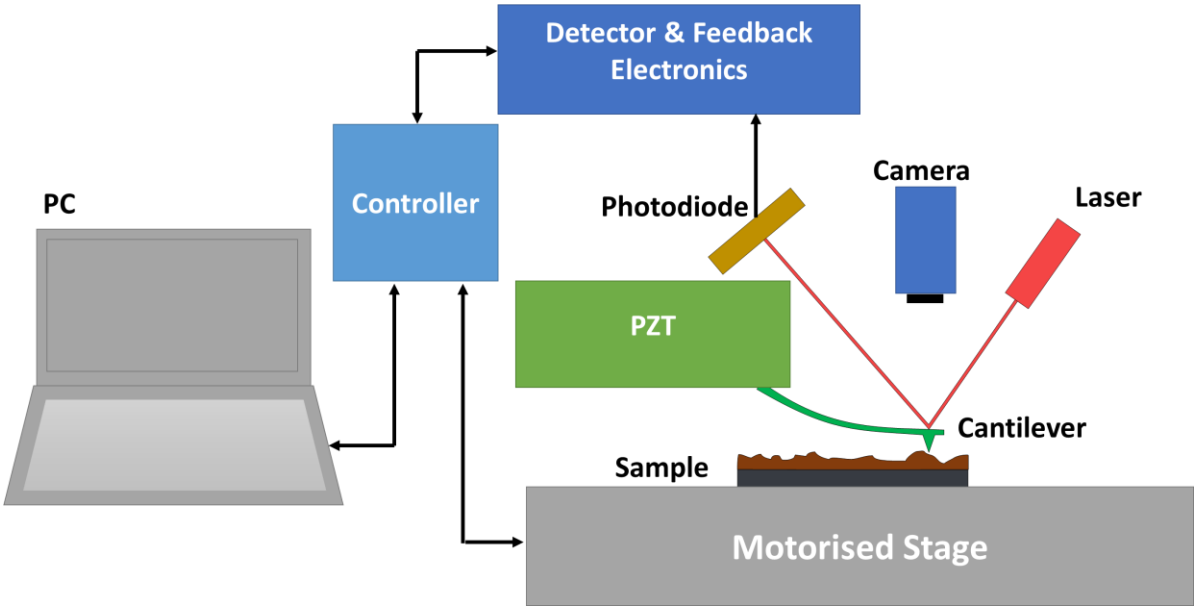


Fig. 3-12: Schematic illustration of the atomic force microscope (AFM)

3.2.3. Surface Profiler

Surface profiler is used for measuring step height of layers during micro/nanofabrication. It consists of a stylus which traverses the surface (as illustrated in Fig. 3-13) and the variation on the surface is recorded and converted into an electrical signal. The profiler used for this research is a Bruker Dektak Suface Profiler.

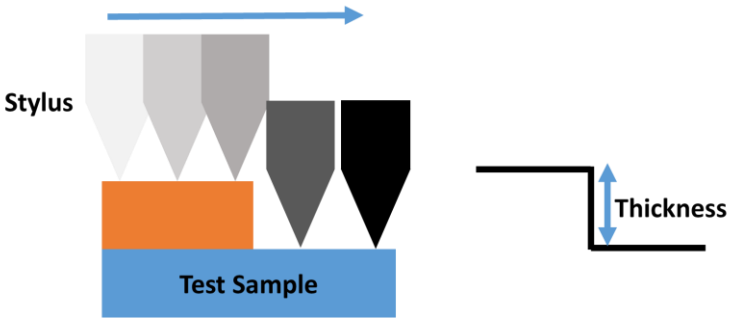


Fig. 3-13: Schematic diagram of surface profiler

3.2.4. Spectroscopic Ellipsometer

Spectroscopic ellipsometry is a non-destructive, non-contact, optical technique. It enables the determination of refractive indices and thicknesses of thin film stacks by measuring the change in polarisation of a probing light beam upon reflection from the sample. The incident light is linearly polarised which when reflected from a surface generates elliptically polarised light. Refractive index, thickness and other surface properties determines the amount of the induced ellipticity. The phase and amplitude relationship between two orthogonal polarisations (p and s waves) are then measured. By fitting with optical models, the thickness, refractive index, interface and/or surface roughness of the film is/are estimated. The J. A. Woolam M2000-XI spectroscopic ellipsometer was primarily

used in this research to measure thicknesses of thin films such as SiO_2, Al_2O_3 on Silicon or SOI wafers as well as flexible substrates using appropriate models.

3.2.5. UV-Vis-NIR Microspectrophotometer

Various suspensions and films were characterised by a Shimadzu UV2600 ultraviolet/visible/near-infrared (UV-VIS-NIR) spectrophotometer with integrating sphere. The transmission and absorption spectrum of various suspensions and films were measured on wavelengths between 200 nm to 1300 nm depending on requirement. Before measurement the baseline was carried out.

3.2.6. Precision Source Measure Unit

For electrical characterisation, either a Keysight B2912A precision source/measure unit (SMU) or a Keysight B1500A semiconductor parameter analyser were used. The former has two SMU channels while the latter has 4 SMU channels as well as two probe Capacitance Measure Unit (CMU). The equipments were used for carrying out current-voltage (I-V) and capacitance-voltage (C-V) characterisation. EasyExpert software was used to operate them.

3.2.6.1. Gate-dielectric characterisation

The gate dielectrics used for various devices (MOS capacitors, MOSFETs of UTC, NWFET) were characterised by comparing experimental CV and theoretically estimated ideal CV graphs. The following section explains this:

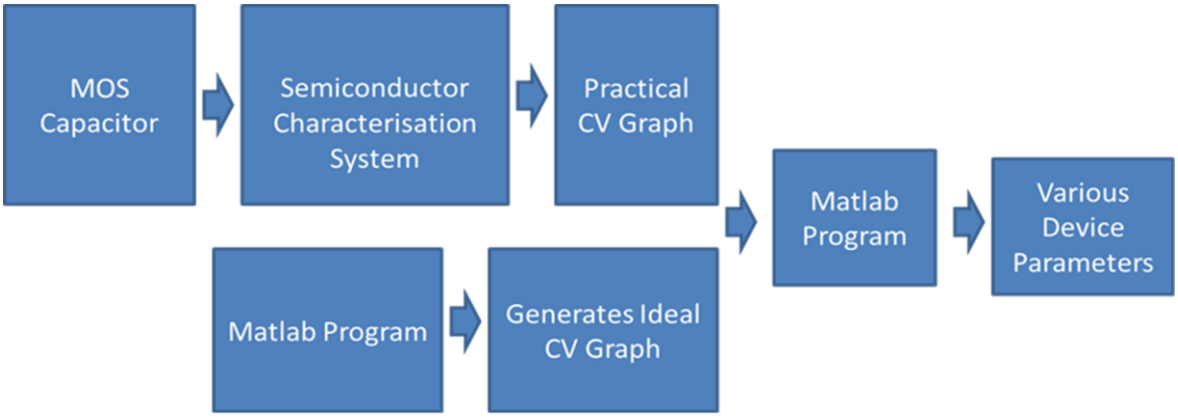


Fig. 3-14: Work flow for characterisation of gate dielectric using CV method.

The following are given as input to the model namely: resistivity of the base wafer, area of the device or diameter of the device, relative dielectric constant and the practical CV graph measured from the MOS capacitor. The MATLAB programme initially calculates the ideal CV graph by solving Poisson's equation.

In order to derive the ideal CV data, the capacitance per unit area of a MOS capacitor is calculated using:

$$C_{total} = \frac{dQ_G}{dV_G} \qquad \textbf{(E 3-4)}$$

Since, to maintain charge neutrality condition, $Q_G = -Q_s$ and applied gate voltage $V_G = V_{ox} + \varphi_s$ i.e. sum of oxide potential and surface potential. Equation ($C_{total} = \frac{dQ_G}{dV_G}$ **(E 3-4)**) can be written as:

$$C_{total} = \frac{-dQ_S}{d(V_{ox} + \varphi_s)} = \frac{1}{-\frac{dV_{ox}}{dQ_S} - \frac{d\varphi_s}{dQ_S}} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s}} \quad \textbf{(E 3-5)}$$

So, total capacitance can be treated as series combination of oxide capacitance and semiconductor capacitance.

While the calculation of oxide capacitance is straightforward ($C_{ox} = \frac{\varepsilon_{ox}\varepsilon_o}{t_{ox}}$), the semiconductor capacitance changes as the surface potential changes during voltage sweep. In general, the charge in semiconductor is represented as the sum of inversion layer charge density Q_{inv}, depletion layer charge density Q_{depl} and accumulation layer charge densityQ_{acc}, which makes semiconductor capacitance as parallel combination of the capacitances arising due to these three types of charges.

$$C_s = -\frac{dQ_S}{d\varphi_s} = -\frac{d(Q_{inv}+Q_{depl}+Q_{acc})}{d\varphi_s} = C_{inv} + C_{depl} + C_{acc} \quad \textbf{(E 3-6)}$$

Using the analytical model expression for the semiconductor charge per unit area Q_S:

$$C_s = -\frac{dQ_S}{d\varphi_s} = C_{so}\frac{\left|1 - e^{\frac{-\varphi_s}{V_T}} + \frac{n_{po}}{p_{po}}(e^{\frac{\varphi_s}{V_T}} - 1)\right|}{\sqrt{2}f(\varphi_s)} \quad \textbf{(E 3-7)}$$

$$f(\varphi_s) = \sqrt{\left[e^{\frac{-\varphi_s}{V_T}} + \frac{\varphi_s}{V_T} - 1 + \frac{n_{po}}{p_{po}}(e^{\frac{\varphi_s}{V_T}} - \frac{\varphi_s}{V_T} - 1)\right]} \quad \textbf{(E 3-8)}$$

$$C_{so} = \frac{\varepsilon_s\varepsilon_o}{L_D} \quad \textbf{(E 3-9)}$$

1D Poisson's equation is then used to solve for electrostatic field and potential under arbitrary bias conditions. The charge density at a distance x from the semiconductor/oxide interface towards bulk is given as:

$$\rho(x) = q(p_{po}e^{\frac{-\varphi}{V_T}} - n_{po}e^{\frac{-\varphi}{V_T}} + N_D - N_A) \quad \textbf{(E 3-10)}$$

Upon integration Poisson equation from bulk to distance x:

$$F^2(\varphi) = \frac{2qp_{po}V_T}{\varepsilon_s\varepsilon_o}\left[e^{\frac{-\varphi}{V_T}} + \frac{\varphi}{V_T} - 1 + \frac{n_{po}}{p_{po}}(e^{\frac{\varphi}{V_T}} - \frac{\varphi}{V_T} - 1)\right] = \pm\frac{\sqrt{2}V_T}{L_D}f(\varphi) \quad \textbf{(E 3-11)}$$

where L_D is the extrinsic debye length given as:

$$L_D = \sqrt{\frac{\varepsilon_s\varepsilon_o V_T}{qp_{po}}} \quad \textbf{(E 3-12)}$$

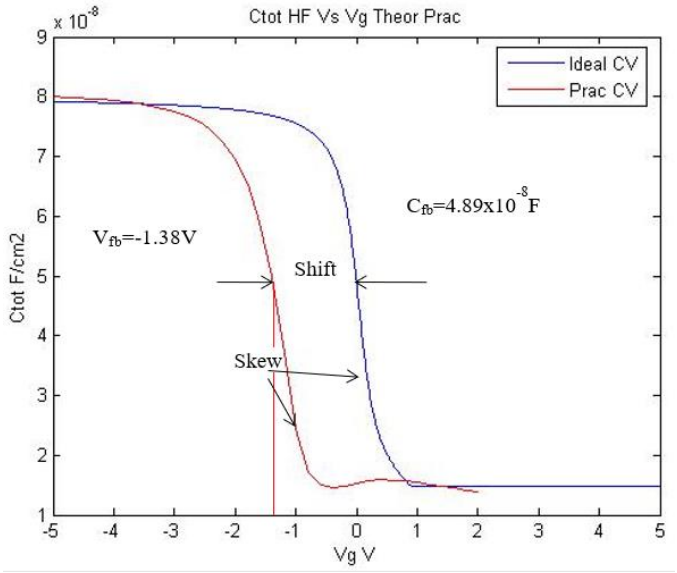
Therefore, at the oxide/semiconductor interface where $\varphi = \varphi_s$, electric field, F_s and total semiconductor charge density, Q_s are given as:

$$F_s = F(\varphi_s) = \pm\frac{\sqrt{2}V_T}{L_D}f(\varphi_s) \quad \textbf{(E 3-13)}$$

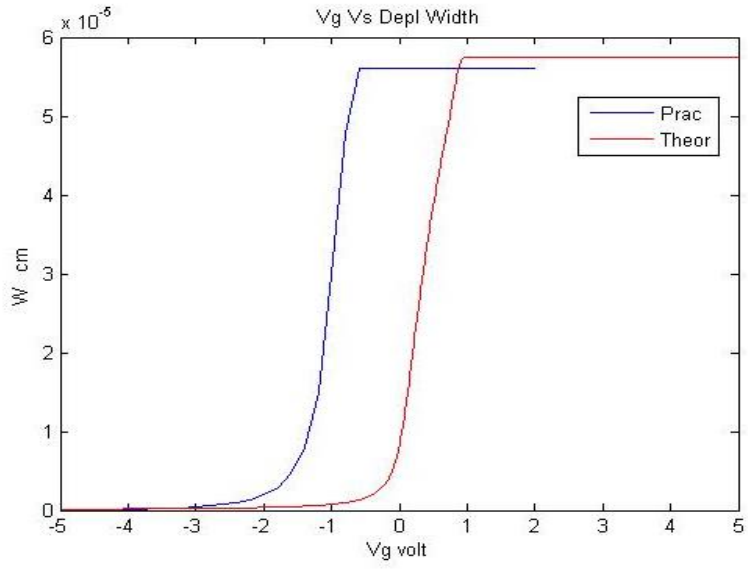
$$Q_s = -\varepsilon_s\varepsilon_o F_s \quad \textbf{(E 3-14)}$$

These equations (E 3-1-E 3-11) were implemented in MATLAB to generate ideal CV. The ideal CV characteristics are compared to empirical CV characteristics to obtain various parameters and characteristics namely, oxide thickness, channel doping concentration, ideal

Vg Vs φ_s , ideal threshold voltage, flat-band capacitance, practical flat-band voltage, oxide charges, doping distribution/profile, practical threshold voltage, Vg Vs depletion width, interface trap density (D_{it}) using LF-HF method and D_{it} using Terman method[234]. Fig. 3-15 shows the comparison of the experimentally measured CV for Al-SiO_2(100 nm)-Si MOSCAP and the theoretically calculated Ideal CV characteristics. The charges in oxide and metal-semiconductor work-function difference causes a shift in the CV characteristics while the interface trap density causes a skew in its CV characteristics compared to the ideal CV. These parameters affect the performance of the fabricated FETs and other devices. Hence it is critical to evaluate in order to engineer high-performance devices.



a



b

Fig. 3-15: (a) Typical experimentally measured (prac in red) CV vs Ideal CV graph (b) Vg Vs depletion width extracted from experimental CV and theoretical estimate (in red)

Table 9: Parameters extracted from a typical CV characteristic shown in Fig. 3-15

Parameters
Ideal Vfb=0V
Prac Vfb=-1.38V
Ideal Vth=0.906V
Prac Vth=-0.48V
φ_{ms} =-0.9215V
Oxide Charges=2.3027x10^{11} Charges
Dit=1.43x10^{11} $cm^{-2}eV^{-1}$
W_{max} =56.128µm

3.2.7. Electromechanical Characterisation

The electrical characteristics of the various fabricated devices (MOS capacitors, MOSFETs etc.) were characterised under mechanical stimulus with the following setups.

3.2.7.1. Three-point Bending

Packed flexible devices or large area devices with electrical leads were tested by mechanically bending them with a 3-point bending setup by Nordson Dage (schematic and photograph shown in Fig. 3-16). The device characteristics were measured under various curvature using this setup.

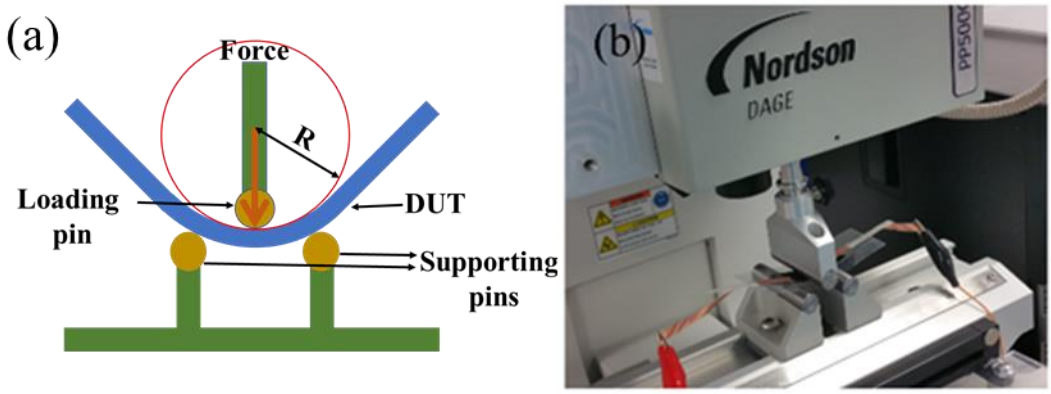


Fig. 3-16: (a) Schematic and (b) image of 3-point Nordson Dage bending setup

3.2.7.1. Testing under Bending Condition on Probe Station

Due to the requirement of large lead electrodes for testing in Nordson Dage, flexible devices in wafer or chip level were tested using an alternate strategy. The devices were carefully mounted on top of 3D printed curved surfaces of different curvatures as shown in Fig. 3-17 and then probed directly.

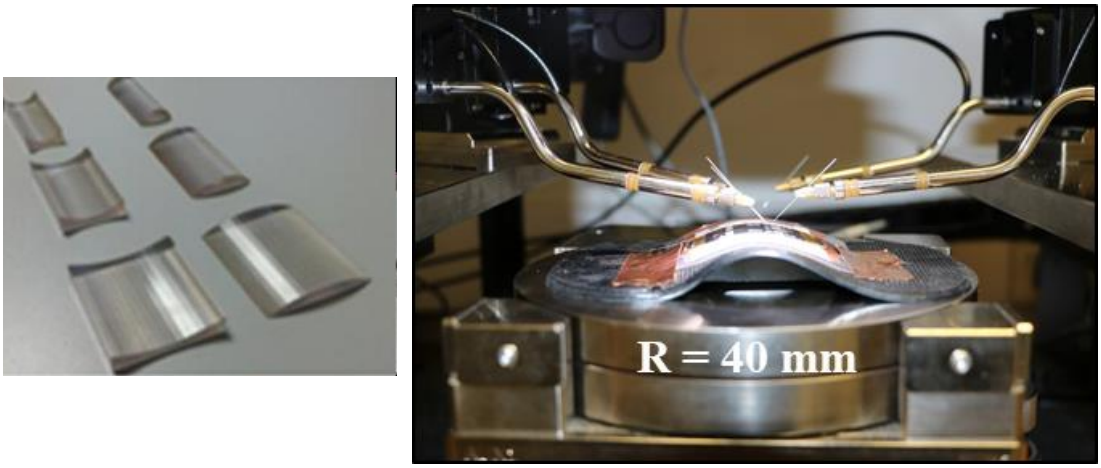


Fig. 3-17: (a) Pictures of 3D printed curved surfaces used for bending analysis (b) Electrical characterisation of samples under bending condition by direct probing [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

3.2.8. Pressure Sensor Characterisation

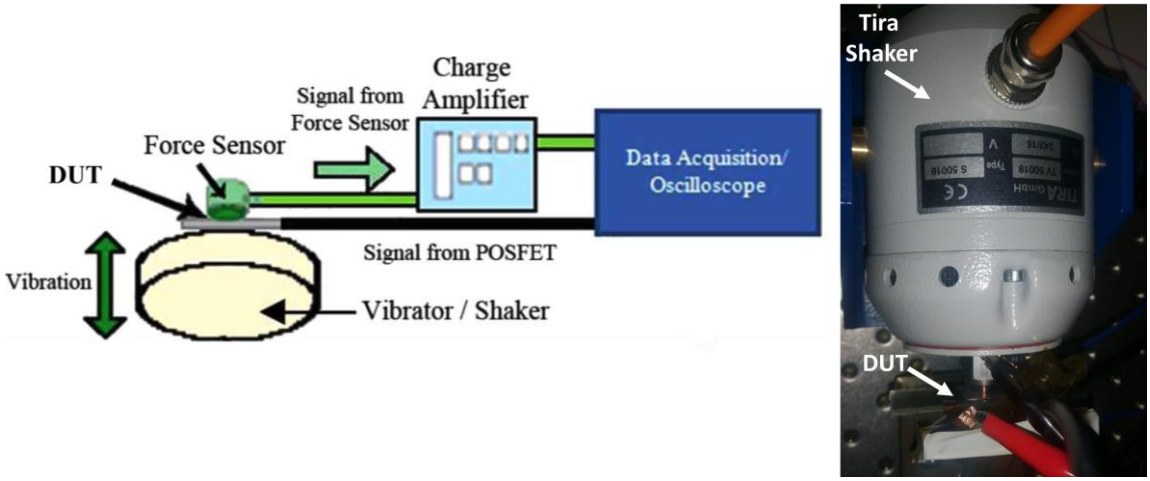
The tactile pressure sensors were tested using two setups as explained below. The fabrication and results of the tactile sensor are presented in chapter 4.

3.2.8.1. Setup for Slow or Static Testing (<2 Hz)

A similar setup to the one used for printing nanowires presented in Fig. 3-11 was used for testing the static tactile sensor (details in chapter 4). Instead of the receiver substrate the sensor was loaded and then pressure applied by moving the vertical linear stage motor controlled by the LabVIEW programme while the applied pressure was measured by precision load cell (Tedea Huntleigh 1004-00.6-JW00-RS). The linear stage motor's movement can be precisely controlled to 1 µm resolution. This was utilised to apply controlled cyclic pulses of force on the sensor of varying amplitude.

3.2.8.2. Setup for Fast or Dynamic Testing (>2 Hz)

The piezoelectric sensor (details in chapter 4) was characterised by a Tira Vibrator/Shaker set up as explained in [42] schematically illustrated in Fig. 3-18. The sensor was firmly placed on the TIRA shaker/vibrator, which is capable of applying dynamic forces of up to 18 N, in a frequency range from 2 Hz to 18 kHz. The shaker is driven by a waveform generator followed by amplifier (TIRA BAA 120). During experiments the sensor was sandwiched between the shaker and a uniaxial PCB Piezotronics force sensor, which measured the dynamic force applied by the shaker. The force sensor has sensitivity of 111 mV/N, a load range of 44.48 N, and a frequency range from 0.01 Hz to 36 kHz.



a b

Fig. 3-18: (a) Schematic illustration of dynamic testing setup (b) Photograph of the Tira Vibrator/Shaker with DUT[235].

3. 3. Simulation Tools

3.3.1. COMSOL Multiphysics

The structural mechanics (Piezoresistivity) module in COMSOL has been used for numerical simulation of the flexible chips. Results including the deformation, stress distribution and electrical resistance in the chip were evaluated for different curvature levels during the test which are now presented in chapter 5. In the model, the silicon membrane has been considered as a piezoresistive material whereas PI has been considered as a linear elastic material.

In the simulation model, the material properties of Table 10 are used for the study of ultra-thin flexible chip. The geometric axis has been subject to orientation rotation to consider the planes of the silicon to be normal to <100> directions.

Table 10: Properties of materials used in analytical model.

Material Property	Silicon	PI (PI2611)
Density	2329 [Kg/m^3]	1300 [Kg/m^3]
Young Modulus	130 [GPa]	8.5 [GPa]
Poisson's Ratio	0.279	0.34
Relative Permittivity	11.7	-
Coefficient of Thermal Expansion (CTE) α	3.2 [ppm/°C]	3 [ppm/°C]

The change in resistivity (ρ) at a given point in the silicon chip is related to the local stress (σ) by the relation:

$$\Delta\rho = \Pi.\,\sigma \qquad \textbf{(E 3-15)}$$

where Π is the piezoresistance tensor (SI units: $Pa^{-1}\Omega m$), a material property. Voigt notation has been employed to feed the values of Π in the COMSOL simulation model. The local current density J is related to the electric field E by the relation

$$E = (\rho + \Delta\rho).\,J \qquad \textbf{(E 3-16)}$$

Other than the electrical calculations, the same equation given below for linear elastic material is also used to solve the structural mechanics of the piezoresistive regions.

The governing equation for the linear elastic material model used in PI is:

$$-\nabla\sigma = \mathrm{F_V} \quad \textbf{(E 3-17)}$$

where σ [N/m^2] is the normal Cauchy stress tensor and is given by

$$\sigma = \mathrm{j}^{-1}\mathrm{FSF}^{\mathrm{T}} \quad \textbf{(E 3-18)}$$

F_V [N/m^3] is the volumetric force vector, F [m] is the deformation gradient tensor, F^{T} [m] is the transposed deformation gradient tensor, S [N/m^2] is the second Piola-Kirchhoff stress tensor, **j** [-] is the determinant of tensor. The deformation gradient tensor is defined as

$$\mathrm{F} = \mathrm{I} + \nabla\mathrm{u} \quad \textbf{(E 3-19)}$$

where I is the identity matrix and ∇u [m] is the material displacement gradient vector.

The anisotropic linear elastic material model is used, including geometric non-linearity, because large deformations are present in the structure and sliding friction is encountered. Furthermore, anisotropic Voigt notation elasticity matrices are used to specify the anisotropic material property of the material. The geometry contains thin components which deform out-of-plane, leading to large deformations. The stress-strain relationship given by Hooke's law is as follows:

$$\mathrm{S} - \mathrm{S}_0 = \mathrm{C}\colon(\epsilon - \epsilon_0 - \epsilon_{\mathrm{inel}}) \quad \textbf{(E 3-20)}$$

where S_0 and ϵ_0 are the initial stresses and strains in the material, C is the elasticity tensor given as input by Voigt matrix notation. Elasticity tensor C [N/m^2] is represented by the Duhamel – Hooke equation and is function of Young's modulus E [N/m^2] and Poisson's ratio ν. The total strain tensor ϵ, as a function of volumetric displacement, u, is:

$$\epsilon = \frac{1}{2}[(\nabla\mathrm{u})^{\mathrm{T}} + \nabla\mathrm{u} + (\nabla\mathrm{u})^{\mathrm{T}}\nabla\mathrm{u}] \quad \textbf{(E 3-21)}$$

3.3.2. Silvaco TCAD

Various processes (oxidation, diffusion) and device (nanowire/ribbon-based JLFET, ν-NWFET) level simulation studies presented in this thesis were carried out using Silvaco TCAD tools [236]. These have the capability to simulate both process and device simulations in one go. Such physically based simulation is needed in order to study the effect of various structure and process parameters in device performance. ATHENA is a comprehensive software tool within the Silvaco TCAD package used for modelling semiconductor fabrication processes. It provides facilities to perform efficient simulation analysis that acts as substitute for costly real-world experimentation. It combines high temperature process modelling such as impurity diffusion and oxidation, topography simulation, and lithography simulation in a single, easy to use framework. This tool comprises within itself SSUPREM4, ELITE and OPTOLITH. ATLAS is the device simulator[236]. The ATLAS device simulator module includes a wide variety of semiconductor physics models for drift-diffusion transport, energy balance, quantum effect, SRH recombination, radiative recombination, Auger recombination, surface recombination, lattice heating, ray tracing, carrier generation, wide range of materials, Fermi–Dirac and Boltzmann statistics, doping effects, trap dynamics, band gap narrowing, tunnelling etc. The simulation results were normally plotted and viewed in the tool TONYPLOT from which they were exported for further analysis.

3. 4. Summary

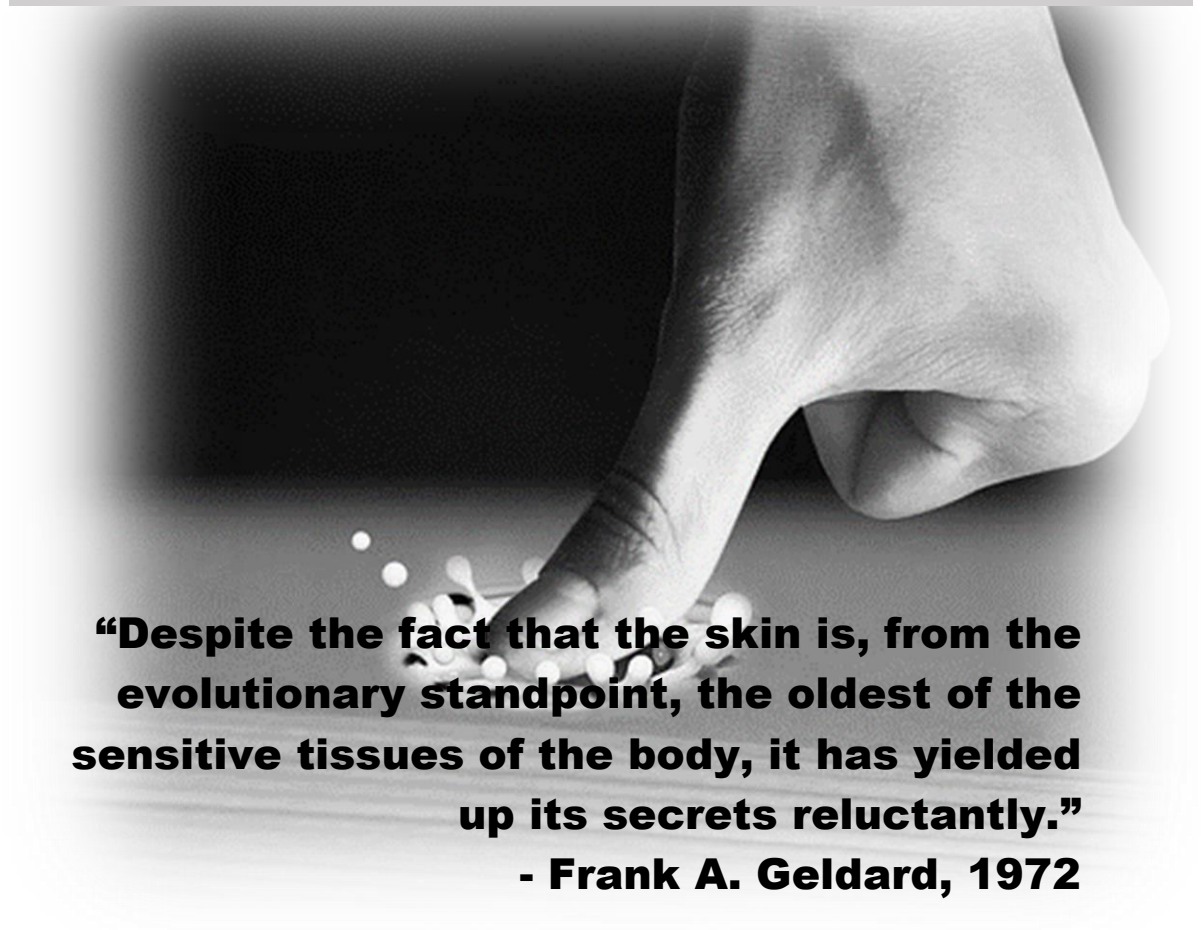
Table 11 summarises the list of various techniques/tools used for this research in terms of processing, characterisation and simulation.

Table 11: Various techniques/tools used for this research

Processing Tools/Techniques	**Characterisation Tools/Techniques**	**Modelling/ Simulation Tools**
Photolithography E-beam Lithography E-beam Evaporation Thermal Evaporation Wet Chemical Etching Reactive Ion Etching Plasma Asher Temperature-assisted Dip-coating Contact Printing Large-area DEP Laser Ablation Patterning Four Probe Technique	Scanning Electron Microscope Atomic Force Microscope Surface Profiler Spectroscopic Ellipsometer UV-Vis-NIR Microspectrophotometer Precision Source Measure Unit LCR Meter Capacitance Measure Unit 3-Point Bending Setup Static Pressure Testing Tira Shaker/Vibrator	Matlab Silvaco TCAD COMSOL Multiphysics SimBrain MultiSim

4

Biomimetic Tactile Sensor



“Despite the fact that the skin is, from the evolutionary standpoint, the oldest of the sensitive tissues of the body, it has yielded up its secrets reluctantly.”
- Frank A. Geldard, 1972

Adapted from

W. T. Navaraj, O. Ozioko, R. Dahiya, "Capacitive-Piezoelectric Tandem Architecture for Biomimetic Tactile Sensing in Prosthetic Hand", IEEE Sensors Conference, 2018, Copyright © 2018, IEEE.

Contents

4. Biomimetic Passive Tactile Sensing Structure

4. 1. Motivation

As presented in **section 2.4.2**, both static (like SA) and dynamic (like FA) sensors are needed to mimic biological tactile sensors effectively to achieve necessary functionalities such as object/texture discrimination, slip detection particularly to obtain information like friction, stickiness, texture, hardness and elasticity[184]. Further, with a transparent sensor, it is possible to realize an energy autonomous sensor as demonstrated with graphene with colleagues [34] . This section presents a biomimetic tactile sensor architecture capable of both static and dynamic tactile sensing. The next chapter shows the results of this interfaced with MOSFET in an extended gate configuration. A system level interface with a prosthesis is presented in detail in the final chapter where this research fits in.

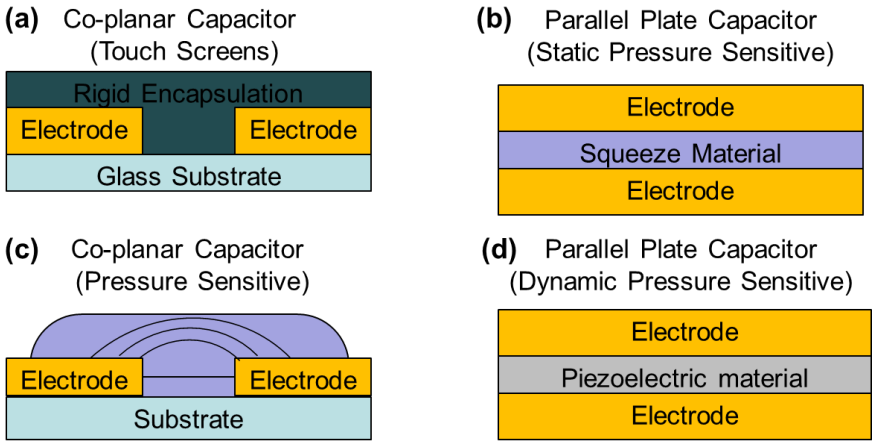


Fig. 4-1: (a-d) Architectures of capacitive tactile sensors

Various architectures are used to realize tactile pressure sensors for electronic skin [34] some of which are shown in Fig. 4-1. The structure shown in Fig. 4-1a is typically used in touch screens where the act of touch with a finger introduces a additional projected capacitance between the two electrodes which is sensed by the sensing electronics [44]. The limitation with this structure is that it can only detect touch and is not pressure-sensitive. Capacitive structures with squeeze film dielectric based approach for pressure sensing is widely used for pressure sensitive electronic skin by various researchers [209,237]. A modified coplanar structure Fig. 4-1c was fabricated along with colleagues to realize a graphene based transparent tactile sensor and further to realize a energy-autonomous electronic skin [34]. Piezoelectric metal-insulator-metal (MIM) structures have also been used by researchers for realising dynamic tactile sensors and e-skin[178].

4. 2. Sensor Architecture

A capacitive architecture in tandem with a piezoelectric structure is used here to realize a tactile sensor as shown in Fig. 4-2. Fig. 4-2a shows the pattern of the three layers of electrodes used for realising the sensor. Fig. 4-2b shows the schematic of various layers of the tactile sensor and Fig. 4-2c shows its equivalent diagram. The work presented here pertains to the implementation of tactile sensing on the distal phalange of the index finger. The sensor structure is integrated with an in-house developed 3D printed prosthetic hand (Fig. 4-2f). When static pressure is applied to the sensor, the elastomer (low-modulus and high-modulus) undergoes compression. This results in the floating electrode (F) coming closer to the signal (S) and ground (G) electrodes. Further, the effective dielectric constant

of the elastomer also changes under compression. As a result, the projected capacitances of the floating electrode onto the interdigitated terminals of signal and ground electrodes (i.e., C_{FS} and C_{FG}) increases. This results in the net capacitance C_{SG} to increase which is read out by a capacitive readout circuit presented in [34]. Compared to a parallel plate capacitive structure, a coplanar structure with a floating electrode is advantageous as there is no output terminal on the top. In the case of the former, the output terminal may break or get damaged due to significant strain on it when objects come in contact with the top electrode. Use of a dual elastomer layer for the capacitive structure is advantageous as during low pressure, the low-modulus elastomer will undergo significantly more compression compared to the high-modulus elastomer. At high pressure, the low-modulus elastomer saturates where the high-modulus elastomer contributes to capacitance change. High speed dynamic forces acting on the piezoelectric layer will cause piezopotential to be generated between the bottom electrode and ground (V_{BG}) as well as signal electrodes (V_{BS})[238]. Here, V_{BG} is used for further processing.

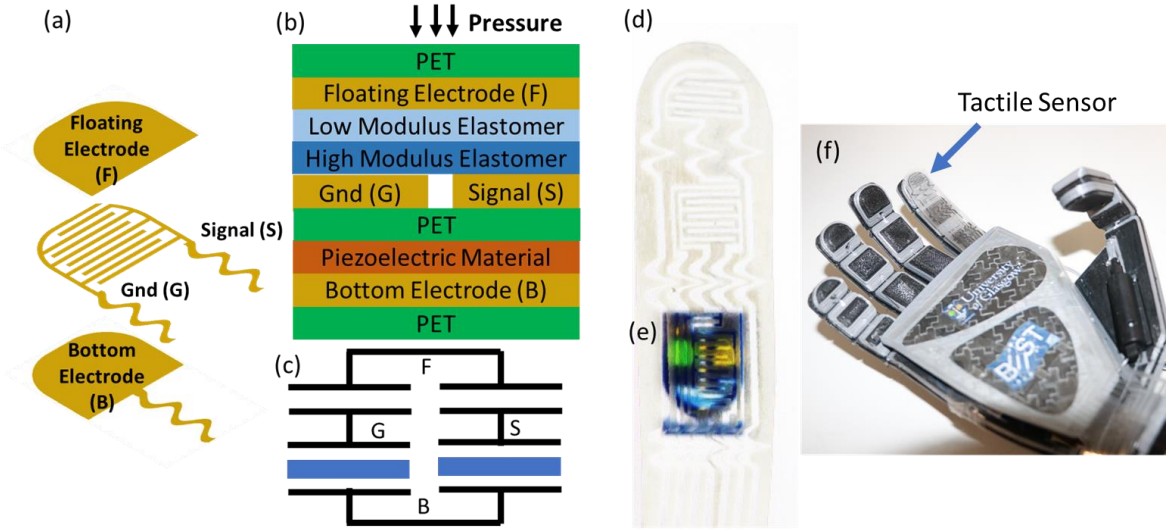


Fig. 4-2: (a) Design of electrodes (b) Stacks of sensing structure (c) Equivalent diagram (d) Fabricated ITO electrodes over which stack was formed showing (e) translucency (University of Glasgow logo on the background) (f) Prosthetic hand with tactile sensor in the index finger [239] Copyright © 2018, IEEE.

The electrode structures were fabricated by a facile approach, which involves laser patterning of sputter-coated Indium Tin Oxide (ITO) film (~70 nm thick) on a Poly Ethylene Terephthalate (PET) substrate ~120 µm thick). As illustrated in Fig. 1-2g, sputtered polycrystalline inorganic film on flexible substrate is suitable for realising flexible electronics. The optimisation of ITO film (sputtered from a Kurt-Lesker sputter target In_2O_3:SnO_2 = 90:10) is presented in Table 12 and the corresponding transmittance spectra of samples are shown in Fig. 4-3 measured with a Shimadzu UV2600 spectrophotometer as explained in section 3.2.5. As the O_2 flow relative to Ar flow was increased the resistivity decreased. While there is no significant difference in the transmittance (>91% normalised transmittance for all) other than some changes arising from thickness variation, the resistivity showed significant variation. Sample C with a resistivity of 3.17 Ω.cm (as measured by four probe technique) is suitable for this application.

A CO_2 laser capable of a maximum power of 60 W was used to ablate the ITO for patterning the electrodes. The sheet resistance of electrodes, measured by a four-point probe, is ~94 Ω/□. The elastomeric layer stacks and piezoelectric films were cut using a blade cutter

as described in [34]. P(VDF-TrFE) co-polymer film (~100 µm) from piezotech FA was cut and bonded between the middle and bottom ITO/PET sheets with thin bonding paste as illustrated in Fig. 4-2b. The ITO sheets and the P(VDF-TrFE) were plasma treated in a radio frequency oxygen plasma system for 2 mins at 150 W before stacking and attaching with a low-stress epoxy adhesive.

Table 12: Optimisation of sputtering parameters

Sample	Ar Flow (sccm)	O_2 Flow (sccm)	Power (watt)	Time (min.)	Inter-electrode distance (cm)	Resistivity $x10^{-4}$ Ω.cm	Normalised Transmitt. %
A	5		100	30	10	1858	93.14
B	4.5	0.5	100	30	10	65.2	91.39
C	4	1	100	30	10	3.17	91.01

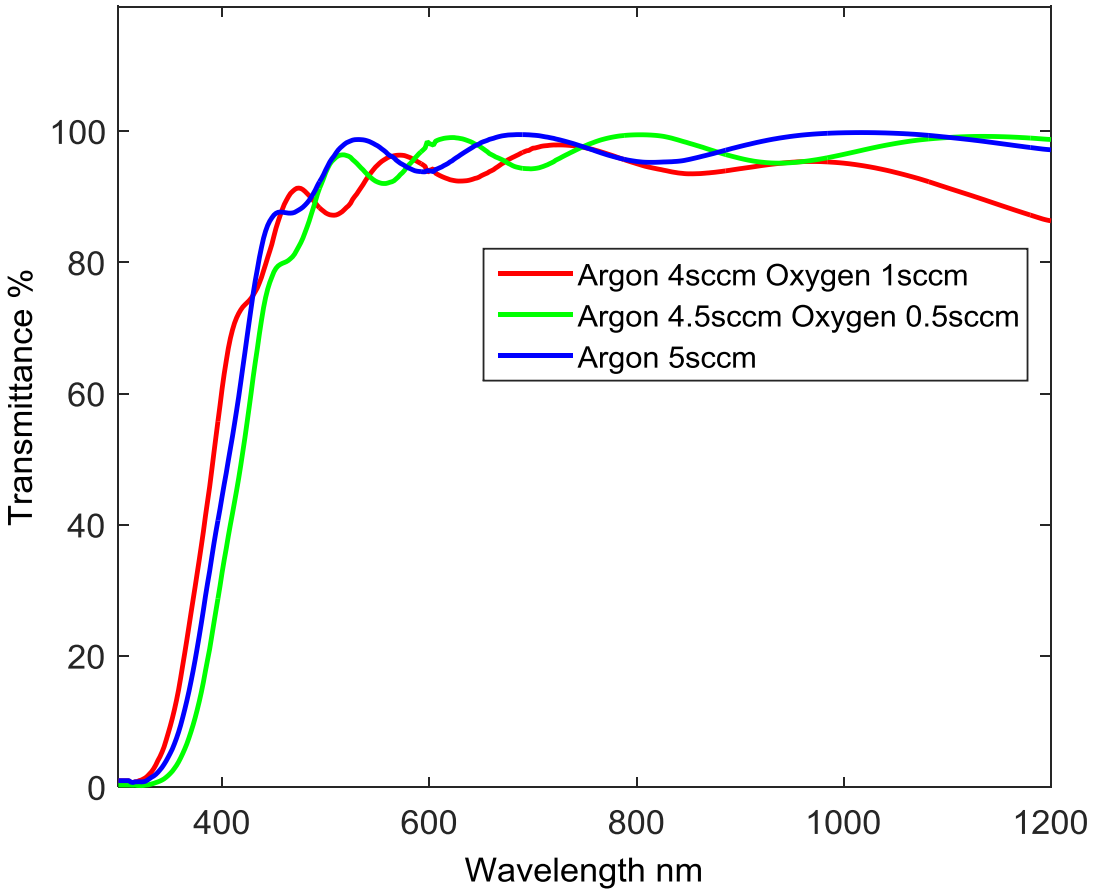


Fig. 4-3: Transmission spectrum of sputtered ITO films.

The high-modulus elastomer was realised by spin coating Sylgard 184 comprising of 10:1 mixture of pre-polymer base and crosslinking agent at a spin speed of 200 RPM resulting in a thickness of (~110±10 µm). EcoFlex™ 00-30 silicone rubber from Smooth-On was used to realize the film for the low-modulus elastomer. It comes as two liquids which were mixed in a ratio of 1:1 and then spun at 200 RPM on top of a PDMS film to get a net thickness (~230±10 µm). The resulting film was partially cured at room temperature for 30 mins and at 80˚C for ten minutes before cutting and transferring it to the laser cut ITO sheet stack. This was partially cured at room temperature for 30 mins before transferring it to the

partially cured PDMS high modulus elastomer film. Fig. 4-2d shows the laser patterned ITO on which the tactile sensing stack was realised.

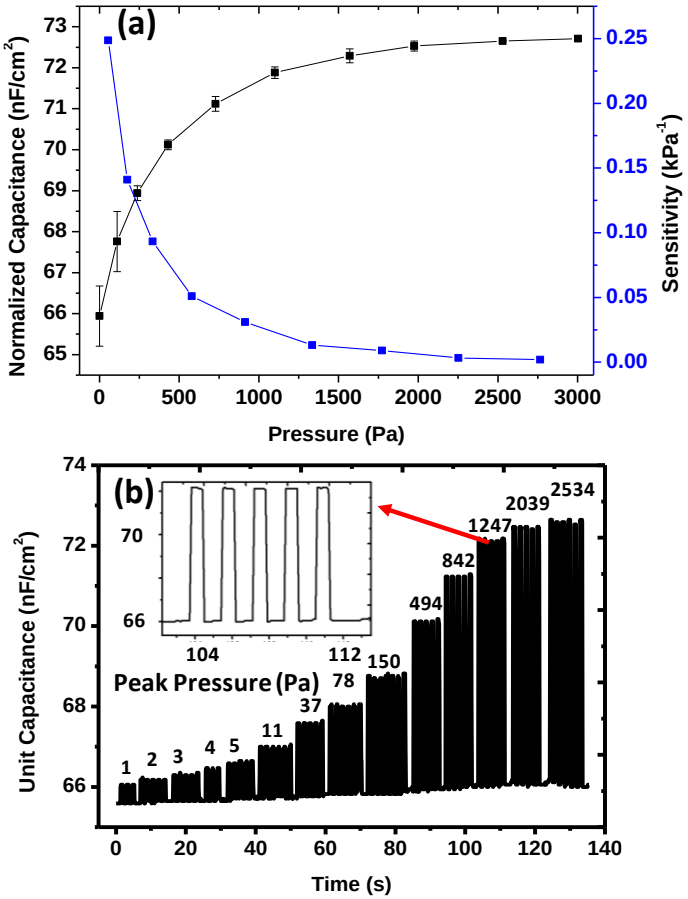


Fig. 4-4: (a) Static Characteristics of the sensor CSG (b) Transient Characteristics (Inset: Zoomed out view of response at peak cycle pressure of ~1.25 kPa) [239] Copyright © 2018, IEEE.

4. 3. Sensor Characteristics

The static pressure sensing performance of the system was evaluated by applying force of varying amplitude using a linear stage motor, controlled via LabVIEW program as explained in section 3.2.8.1. This was utilised to apply controlled cyclic pulses of force on the sensor of varying amplitude. The capacitive sensor was tested by measuring the capacitance using Keysight E4980AL Precision LCR Meter while force value was recorded from a loadcell. Fig. 4-4 shows the output of the two types of tactile sensing structure. The static capacitive sensor's characteristic C_{SG} shown in Fig. 4-4a was found to be non-linear with very high sensitivity (up to 0.25 kPa^{-1}) in the lower pressure (<100 Pa) range while lower sensitivity in higher pressure (0.002 kPa^{-1} at ~2.5 kPa). It is to be noted that the tactile mechanoreceptors in the human hand also exhibit non-linear response with similar sensitivity variation qualitatively [240]. The transient characteristics of the same capacitive structure is shown in Fig. 4-4b.

Assuming the fringe capacitance between the interdigitated electrodes of capacitance C_{SG} is negligible, the C_{SG} is related to C_{SF} and C_{FG} as:

$$\frac{1}{C_{SG}} = \frac{1}{C_{SF}} + \frac{1}{C_{FG}} \qquad \textbf{(E 4-1)}$$

Assuming, normalised unit areal capacitance with symmetry ($C_{Norm-SF} = C_{Norm-FG}$) which is related to normalised low modulus ($C_{Norm-LME}$) and high-modulus ($C_{Norm-HME}$) unit areal capacitances as:

$$\frac{1}{C_{Norm-SG}(P)} = \frac{2}{C_{Norm-FG}(P)}$$

$$= 2\left(\frac{1}{C_{Norm-LME}(P)} + \frac{1}{C_{Norm-HME}(P)}\right) \quad \textbf{(E 4-2)}$$

$$C_{Norm-XME}(P) = \frac{\varepsilon_0 \varepsilon_{XME}(P)}{2\left(d_{0-XME} - {}^{Pd_{0-XME}}/_{Y_{XME}}\right)} \quad \textbf{(E 4-3)}$$

Where, ε_0 is the permittivity of free space, $\varepsilon_{XME}(P)$ is the effective relative dielectric constant of the low or high modulus elastomeric stack under pressure, d_{0-XME} and Y_{XME} are the initial thickness and the Young's modulus of the particular elastomeric stack, respectively. The above equations imply an increase in capacitance under pressure as observed in Fig. 4-4.

The piezoelectric sensor was characterised by a Tira Vibrator/Shaker set up as explained in section 3.2.8.2. The voltage output V_{BG} of the piezoelectric stack at 10 Hz input of various peak pressure amplitudes (in Pa) is shown in Fig. 4-5a. Fig. 4-5b shows peak voltage vs peak pressure amplitude of the sensor. The force applied to piezoelectric transducer results in a net dipole moment within the piezoelectric material due to non-centrosymmetric property of the material, resulting in piezo-potential generation. The relationship between applied force and charge generated can be approximately described as[241]:

$$Q = d_{33}F \quad \textbf{(E 4-4)}$$

Where, d_{33} is the piezoelectric coefficient and F is the applied force. As the generated charge density is linearly dependent on the applied pressure (force per unit area), the generated piezo-potential is directly dependent on the magnitude of the pressure. Thus, a higher magnitude of force/pressure results in higher magnitude of piezo-potential. The piezoelectric sensor structure exhibited a sensitivity of 2.28 kPa^{-1}.

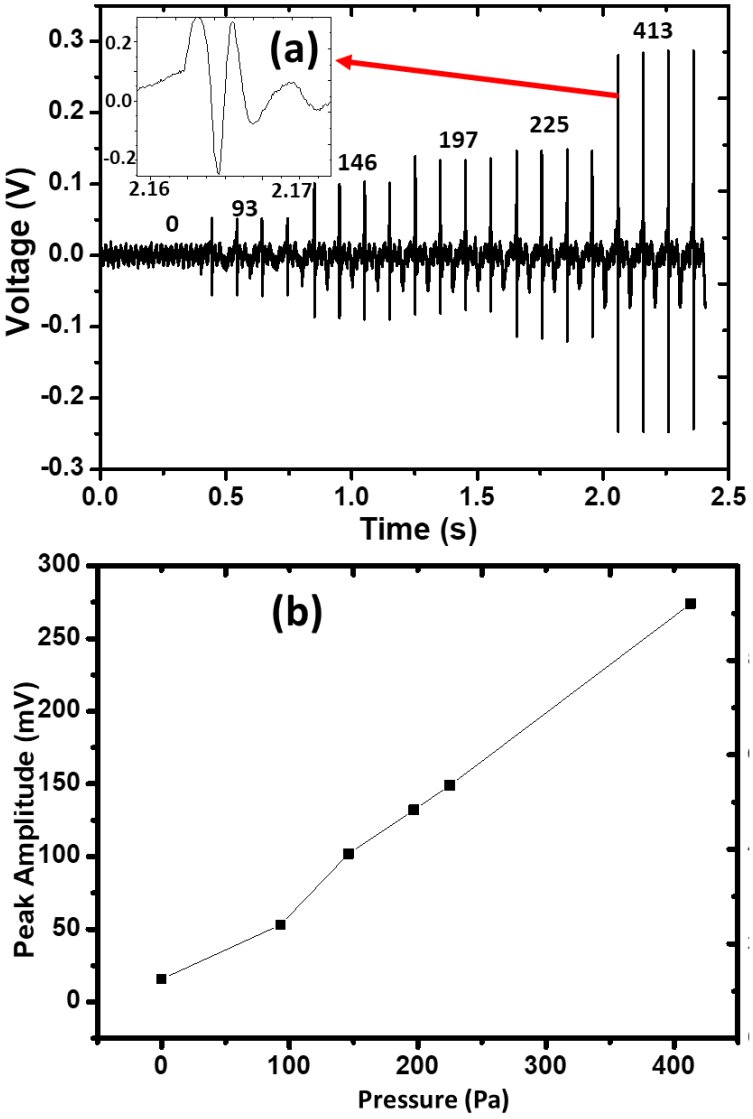


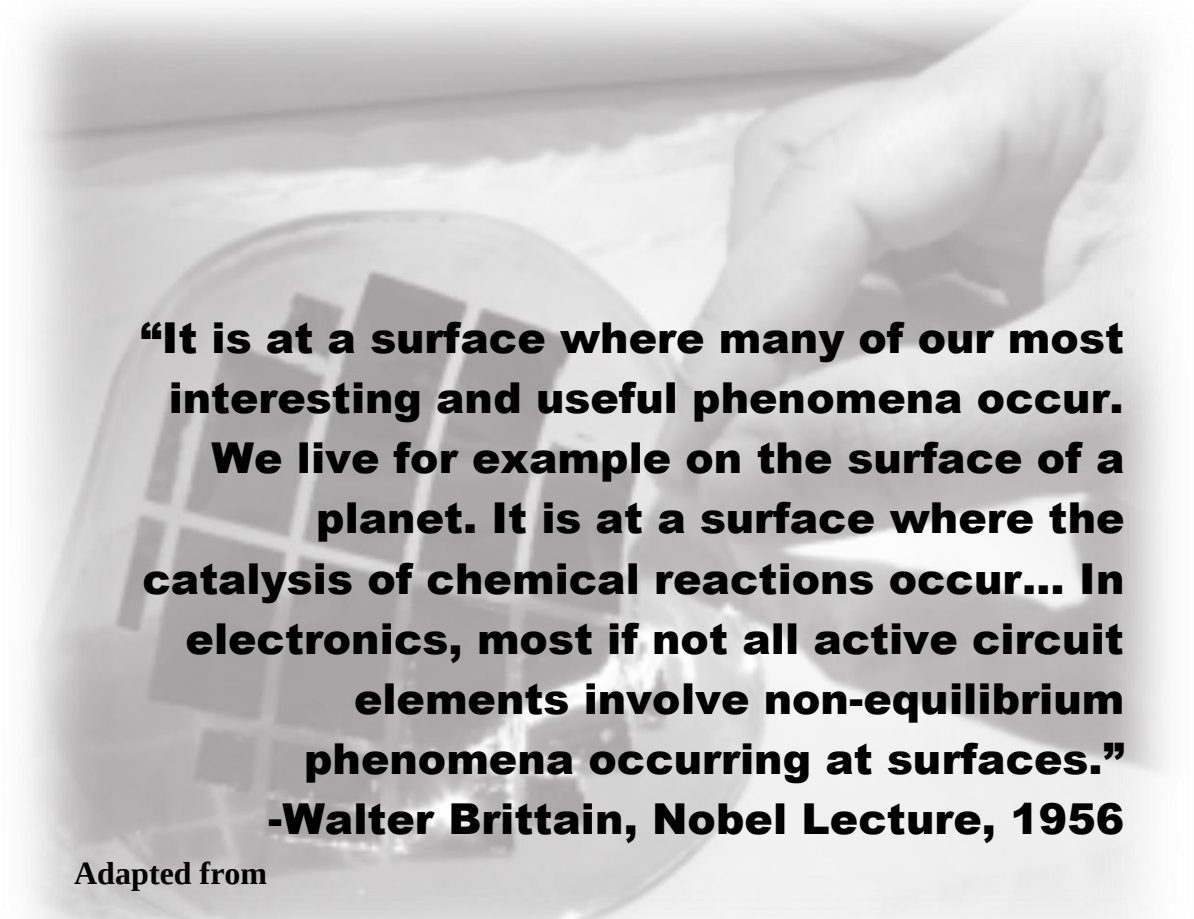
Fig. 4-5: (a) Transient Characteristics of the piezoelectric structure V_{BG} (Inset: Zoomed out view of response at peak cycle pressure of ~413 Pa) (b) Peak force Vs corresponding peak output amplitude. [239] Copyright © 2018, IEEE.

4. 4. Summary

The approach presented in this chapter to realize sensory structure in a facile strategy with dynamic and static sensing capability is attractive for prosthetic and robotic tactile sensing. The non-linearity of the capacitive structure with higher sensitivity (0.25 kPa^{-1}) at low pressure range (<100 Pa) is desirable provided the sensor responds for broad pressure range. The piezoelectric sensor though on the base of the stack exhibited a linear response with sensitivity of 2.28 kPa^{-1}. The goal is not to develop a advanced sensor but a sensor structure to test the proposed IMNS concepts. The next chapter shows the realisation of bendable MOSFET and how the MOSFETs are interfaced with these sensors in an extended gate configuration. A system level interface with a prosthesis is presented in chapter 8 of this thesis.

5

Ultrathin Wafers and Chips



“It is at a surface where many of our most interesting and useful phenomena occur. We live for example on the surface of a planet. It is at a surface where the catalysis of chemical reactions occur… In electronics, most if not all active circuit elements involve non-equilibrium phenomena occurring at surfaces.”
-Walter Brittain, Nobel Lecture, 1956

Adapted from

W. T. Navaraj, S. Gupta, L. Lorenzelli, and R. Dahiya, "Wafer Scale Transfer of Ultra-thin Silicon Chips on Flexible Substrates for High-performance Bendable Systems," Advanced Electronic Materials, p. 1700277, 2018, © 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Contents

5. Ultra-thin Wafers and Chips

Silicon-based micro/nanoelectronics technology has been playing a vital role in consumer electronics industry as various breakthroughs helped to bring the device dimensions down to nanoscale and exponentially scale the device densities up to billions of devices per cm^2. This is an obvious choice as potential candidate for high-performance flexible electronics as well, especially where large scale integration is required. In the current work, wafer-scale transfer printing of ultra-thin chips from bulk wafer was carried out with functional electronics including MOS capacitors and MOSFETs. This transfer process is key to achieve large scale tactile sensors using micro/nanoelectronics technology. This chapter presents the work done in realising silicon-based ultra-thin wafers and chips for high-performance flexible electronics and its application in realising extended gate active tactile sensors.

This chapter is organised as follows: The sample fabrication and methodology for wafer thinning and wafer scale transfer of UTCs is presented in Section 5. 1. This has been demonstrated with the transfer of various samples obtained with increased fabrication complexity. These include ultra-thin silicon resistive membranes, MOS capacitors (MOSCAP) and n-channel MOSFETs. These devices have been characterised in detail in Section 5. 2. to evaluate the effectiveness of proposed methodology. The analysis includes finite element modelling, estimation of critical bending, electro-mechanical characterisation and bending induced deviations in basic electrical parameters of devices on thin Si. The changes in material properties like transmittance and surface morphology have also been studied to understand the new avenues UTCs offer in terms of applications. Finally, piezoelectric sensors and capacitive sensor presented in the previous chapter were used in extended gate configuration with the MOSFETs to form active tactile sensors as explained in Section 5. 3.

5. 1. Fabrication of UTCs and Transfer Methodology

As presented in section 2.2.1, Si wafers start to lose their rigidity when they are thinned down to around 150 µm[88]. Below 50 µm they get more flexible, and below 10 µm the Si membrane starts to become optically transparent[47]. Using a combination of pre/post-processes steps a few solutions for chip-scale fabrication of UTCs have been reported in the literature[88,242]. At wafer scale, the methods that have been explored largely include mechanical grinding from backside of bulk[47] as well as SOI[243] wafers with a combination of wet and dry etching processes. Mechanical grinding is a costly step and there is a risk of development of micro-cracks in the chips during grinding. The SOI wafers-based approach is relatively free from the micro-crack issue, but the cost concern remains as the SOI wafers are generally expensive than bulk wafer by an order of magnitude. A few recent methods for UTCs include controlled spalling technique for wafer scale transfer of integrated circuits from SOI wafers[244,245] or mechanical exfoliation of transistors from bulk wafers[246]. The mechanical exfoliation process is known to increase the gate leakage current, which degrades the electrical performance of devices. A combination of deep reactive ion etching (DRIE-BOSCH) process and isotropic etching has been used to achieve semi-transparent high-performance flexible electronics from bulk Si at an area of 3.75 cm^2 (2.5 cm×1.5 cm)[247]. A similar process has been used to realize flexible dies (comprising FinFETs) with an area of 7.5 cm^2 (2.5 cm×3 cm)[248]. The cost associated with DRIE and the loss of wafer area because of holes needed for release of the top layer make it difficult to use this process for high density integrated circuits. Compared to these methods, wet etching is relatively less costly and free from the issues of micro-cracks. Since the active

layer remains unaffected during backside etching, there is no adverse impact on device response after etching. The method presented in this chapter is based on the chemical thinning of wafers down to ~15 µm and then transferring the UTCs to flexible polyimide[132,40,22]. The transfer printing that has thus far been used to transfer quasi 1-D micro/nanostructures such as nanowires or ribbons to flexible substrates has been extended here for the first time to achieve wafer-scale transfer of UTCs[132,40,249,58].

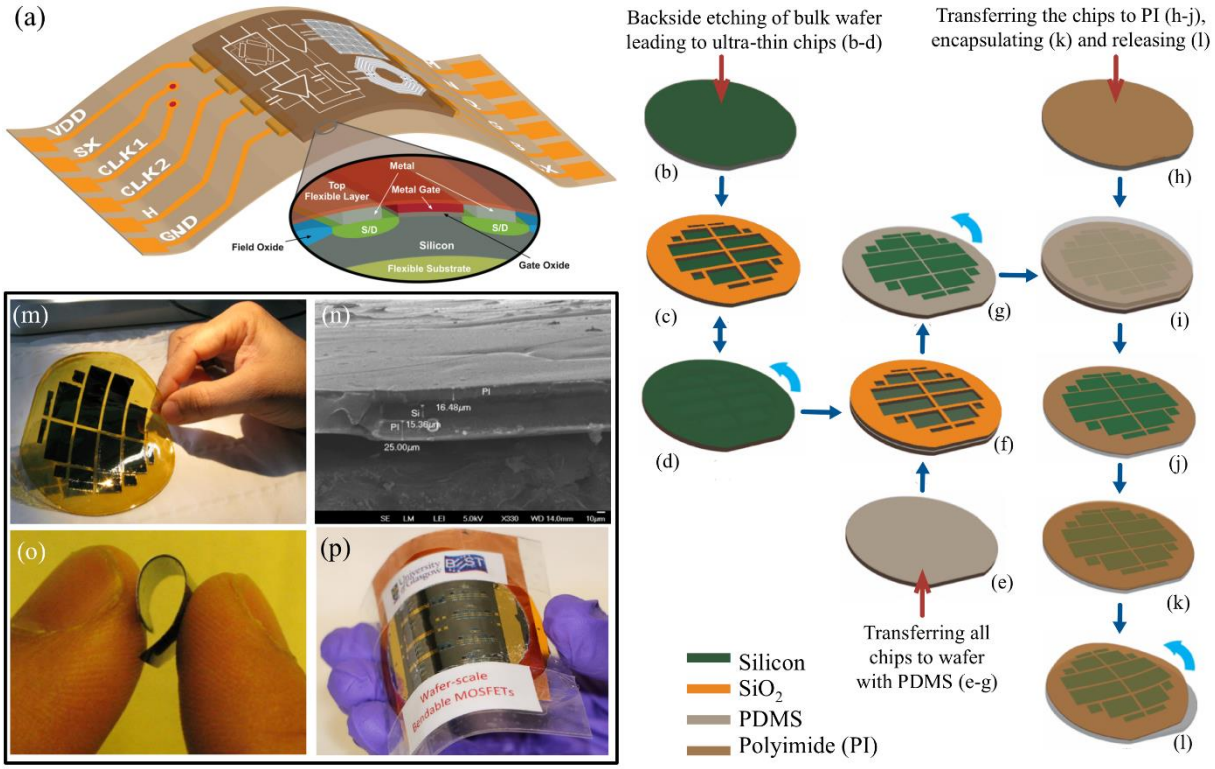


Fig. 5-1: a) The scheme of UTCs with integrated multi-materials stack on foil. b-l) The process flow of fabrication and wafer scale transfer of UTCs to flexible polyimide: (b) Initial wafer. (c) the back and, d) front of the wafer after chemical etching. e) A temporary second wafer spin coated with ~ 200 µm thick PDMS. f) The wafer with thin Si chips placed on the second wafer. g) Laser cutting of the top wafer on PDMS to remove the bulk Si, leaving behind the UTCs on the second PDMS coated wafer. h) A third temporary wafer with final substrate (~15µm thick polyimide). i) Bonding of the second wafer (after UTCs transfer) with the third wafer. j) Chemical etching of PDMS to remove the second wafer. k) Spin coating another layer of polyimide to encapsulate the UTCs. l) The final wafer-scale UTCs released from the third wafer; m) Image of the transferred UTCs. n) The cross-sectional SEM image of Si chips encapsulated in polyimide. o) The bending of bare Si chip and, p) MOSFET laminated between PVC sheets. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

The post-processing steps shown in Fig. 5-1**(c-l)** follow the fabrication of devices on the top of silicon.

4" p-type, double side polished Si wafers (resistivity 10-20 Ω-cm) were used in this study. Initially the ultra-thin resistive structures were fabricated, and transfer printed. The pre-processing step used for achieving the UTC involves thermal growth of SiO_2 on the rear side of the wafer and patterning it to act as hard mask for chemical etching during post-

processing as shown in Fig. 5-1**(c-d)**. UTCs of various sizes (0.5 cm x 0.5 cm; 0.5 cm x 1.5 cm; 2.0 cm x 1.5 cm; and 3.5 cm x 1.5 cm) were obtained by BOE etching of photolithography defined patterns on rear side. The defined patterns considered the dimensional corrections needed due to anisotropic etching with TMAH. The resistive elements were realised from phosphorus doped (~$10^{16}/cm^3$) wafers. The doping, achieved through ion-implantation on the front side, led to a shallow n-junction of ~0.5 µm depth. Then the wafers with resistive elements were carefully mounted on a teflon jig with a double O-ring system to seal the devices on the front side from getting attacked by the etching chemical, while the rear side is open for the chemical to etch. After this, the chemical etching of the wafer was carried out using 25 wt% TMAH (Tetra-methyl-ammonium Hydroxide) solution. The etching was carried out until the thickness of wafer reached around 15 µm. At this stage, the thinned portion of wafer can be termed as silicon membranes. During the etching process the thickness of wafer was monitored using profilometer and ex-situ inspection. In principle, etching for longer time could further reduce the thickness of Si membranes. However, due to thickness tolerance related variations in the wafers it is challenging to obtain Si membranes with thicknesses below 10 µm. The jig was carefully raised from the TMAH solution once the etching process is complete. The doping-controlled etching could be exploited to control the thickness of the membranes. As an alternative, SOI wafers could also be used to obtain thinner membranes as the etching process will be stopped by the buried oxide, which is typically 2-3 µm below the top surface.

After chemical etching, the transfer of UTCs on to flexible PI substrate was carried out following the steps shown in Fig. 5-1**(e-l).** With front side down, the membranes were adhered to a carrier substrate which is a ~200 µm thick PDMS (Poly dimethyl siloxane) spin coated on another temporary wafer. The adhesion of membranes with PDMS was controlled by a low power plasma. The wafer was then diced around the thinned regions and the bulk Si was removed, leaving behind the Si membranes on PDMS. This wafer-scale transfer step results in the front-sides of UTCs facing towards PDMS. To gain access to the front side, the membranes were transferred once again to the final receiving substrate i.e. polyimide foils. The polyimide foil was obtained by spin coating PI2611 (from HD Microsystems) on a temporary glass wafer and curing it for 30 minutes at 350°C. The glass wafer was used here because of polyimide's poor adhesion with glass, which allows easy release of foils after the transfer process is completed. An adhesion promoter (VM652 from HD Microsystems) was used at the edges of the wafer to temporarily hold the polyimide on glass wafer[250,88]. Another thin polyimide layer, spin coated over the cured polyimide foil, acted as adhesive during the transfer of UTCs from PDMS to polyimide. The polyimide is used in this work as the final substrate due to excellent features such as high glass transition temperature and good thermal and dimensional stability. These features enable a finer interconnection pitch, better reliability and compatibility with existing semiconductor technology. The PI2611 has the coefficient of thermal expansion (CTE) of 3 ppm/°C, which matches that of Si (3.2 ppm/°C). This matching of thermal coefficients prevents thermal stress build up in the UTCs during curing of polyimide as well as any residual bending thereafter. The temporary wafer having membranes on PDMS was then placed on polyimide film and soft baked in vacuum at 110°C for one minute, leaving the membranes sandwiched between polyimide and PDMS. Following this the PDMS was removed by dissolving it in a dilute solution of Tetra Butyl Ammonium Fluoride (TBAF) in a hydrophobic non-hydroxylic aprotic solvent such as Propylene Glycol Methylether Acetate (PMA)[21]. This completes the wafer-scale transfer of UTCs on polyimide. The UTCs can be encapsulated by spin coating another polyimide layer on the top of transferred UTCs or using hot

lamination method. This process was followed to obtain various devices (**Table 13**) including MOSCAPs and n-channel MOSFETs. As an alternative to above process, a si wafer with thermally grown SiO_2 on the front side can also be used as the second temporary wafer. The latter two temporary wafers could be mechanical grade as they are used only for transfer purpose. For the same reason, they could be reused to improve the cost effectiveness of the process. In the worst case, when all 3 wafers are prime grade and are all consumed in one transfer process the total cost will be ~$150 (considering the typical cost of a 6-inch prime grade Si wafer is ~$50). However, if the two-temporary wafer are mechanical grade (cost ~$20/wafer), this total cost will come down to ~$90. If the temporary wafer can be reused (as proposed here) then the cost will further reduce to ~$50. This is much lower than the typical cost of SOI wafer (~$1000 per 6-inch wafer) used in other approaches.

The MOSCAPs and MOSFETs were fabricated on 2" p-type 1-10 Ohm-cm, <100> Si wafers. For MOSCAP, 100 nm thick high-quality silicon dioxide was grown via dry oxidation at 1000ºC. Nickel (10 nm) and gold (100 nm) were evaporated by electron beam evaporation system and patterned to define the top electrode. A single MOSCAP has an area of 0.48 cm^2. For MOSFETs, a 5-mask-process was used which is schematically summarised in **Fig. 5-2(b1-b8)**. A field oxide of ~0.5 µm was grown on the top of the wafer which was later used to isolate diodes of adjacent MOSFET as well as a hard mask in the rear to protect support boundaries during latter thinning. Lithography was carried out after patterned oxide layer in the front side and the exposed area was etched. Phosphorus was then diffused at 970˚C for 30 minutes through the opened window for creating source and drain region of the transistor as illustrated in **Fig. 5-2(b2)** targeting a junction depth of ~0.5 µm with measured sheet resistance of ~7.4 Ω/□. After defining the active region, a high quality thin oxide of ~100 nm was grown. The contacts holes for diodes were opened through gate oxide itself and metal stack of Ni/Au (10 nm/100 nm) was evaporated. In last stage of fabrication, metal was patterned to define the contact pads and interconnection and sintered in forming gas at 450ºC to get better ohmic contact. The gate length was of 10 µm (with further 5 µm overlap on each diode regions) and channel width of 100 µm. The front sides of wafer were protected from etchant (i.e. TMAH) by ProTEK B3 protective coating from Brewer Science and a custom wafer holder with double o-ring. After fabrication of the devices, ProTEK B3 primer was spin-coated on the front side at 1500 rpm for 30 s with an acceleration of 10000 RPM/s. Then the wafers were baked on a hotplate at 140˚C for 120 s followed by 205˚C for 5 minutes in a convection heating oven. Following the step, the ProTEK B3 protective coating was spin-coated on the front side at 1500 rpm for 60 s with an acceleration of 10000 RPM/s. The wafers were then baked on a hotplate at 140˚C for 120 s and at 205˚C for 30 minutes in a convection heating oven. For further protection, the wafer was placed in a holder with double o-ring. After chemical thinning from rear side (**Fig. 5-2**d), the front ProTEK protection mask was removed by repeatedly rinsing it in fresh acetone and methanol for 4 times until the solution becomes clear. Then, the wafer-scale transfer method **(Fig. 5-2**e-l) was carried out to obtain the UTCs on polyimide. Before transferring the samples, the central section of polyimide was removed to expose the back contacts. After transferring to polyimide, copper tape (50 µm thick) was used as back contact of devices. The tape also serves as the thermal dissipation layer, which is needed for high-performance computing. Instead of using polyimide, the hot lamination of PVC was used to encapsulate the MOSFETs. To gain access to contact pads the openings were cut on the top of the PVC using Silhouette cutter before laminating the devices.

Table 13: Various samples used for bending, optical and electrical analysis with their key specifications

Sample ID.	Structure	Width [cm]	Length [cm]	Si Thick-ness [µm]	Key Parameters
RBC1	Si membrane with free ends	1.5	0.5	~15	Critical theoretical (R_{BC}): 1.097 mm R_{BC} (Expt.) : <1.1 mm
RBC2	Si membrane with two ends anchored using conductive paste	1.5	0.5	~15	Critical theoretical (R_{BC}): 1.097 mmR_{BC} (Expt.) : <1.19 mm
RBC3	Si membrane encapsulated in polyimide and the two ends anchored using conductive paste	2.0	1.5	~15	Transferred to 25 µm thick polyimide (PI) and encapsulated with 16.48 µm thick polyimide on top **Critical theoretical (R_{BC}):** 1.1428 mm with 25 µm/15.36 µm/16.48 µm PI_{Top}/Si/PI_{Bot} concave up and 1.437 mm when concave down R_{BC} (Expt.) :<1.475 mm
UVN1	Thin Silicon	2.0	2.0	15	Net Vis. Transmittance (390 to 700nm) %: 0.170 Net Transmittance (300 to 1100nm) %: 8.694
UVN2	Thin Silicon	2.0	2.0	30	Net Vis. Transmittance (390 to 700nm) %: 0.011 Net Transmittance (300 to 1100nm) %: 8.380
UVN3	Thin Silicon	2.0	2.0	75	Net Vis. Transmittance (390 to 700nm) %: 0.000 Net Transmittance (300 to 1100nm) %: 6.090
UVN4	Bulk Silicon	5.1 φ*	-	300	Net Vis. Transmittance (390 to 700nm) %: 0.000 Net Transmittance (300 to 1100nm) %: 0.927
MOSCAP	MOS Capacitors on p-Si (Wafer scale transfer to polyimide and laminated with PVC)	5.1 φ*	-	~15	Specifications - Au/Ni 100 nm/10 nm as Gate; Oxide Thickness: 100 nm; Si Thickness: ~15 µm; Al 100 nm back metal; Area 0.48 cm^2; Encapsulated with 100 µm PVC lamination with Cu backing
MOSFETs	n-MOSFETs on wafers (Wafer scale transfer to polyimide and laminated with PVC)	5.1 φ*	-	~15	Specifications - Au/Ni 100 nm/10 nm; Oxide thickness: 100 nm; Si thickness: ~15 µm; Channel Length x Width: 10 µm x 100 µm; Al 100 nm back metal; Encapsulated with 100 µm PVC lamination with Cu backing; **Saturation Mobility:** Zero Bending: 350 cm^2/V-s; Tensile Bending: 384 cm^2/V-s; Compressive Bending: 333 cm^2/V-s

***** Indicates Diameter

The proposed methodology for wafer-scale transfer of UTCs has many advantages including compatibility with conventional CMOS process for mass-production. Besides this the proposed method allows easy integration of UTCs on PI foil because steps such as metallisation (e.g. for extended contact pads) can be easily performed on the wafer itself i.e. before releasing the UTCs. Further it is possible to cut and paste the UTCs on any substrate to enable products with heterogeneous integrated systems-on-foil[88,250,251]. The easy handling UTCs and thin wafers can increase the production yield. The methodology does not require sophisticated instruments such as precise pick and place tools.

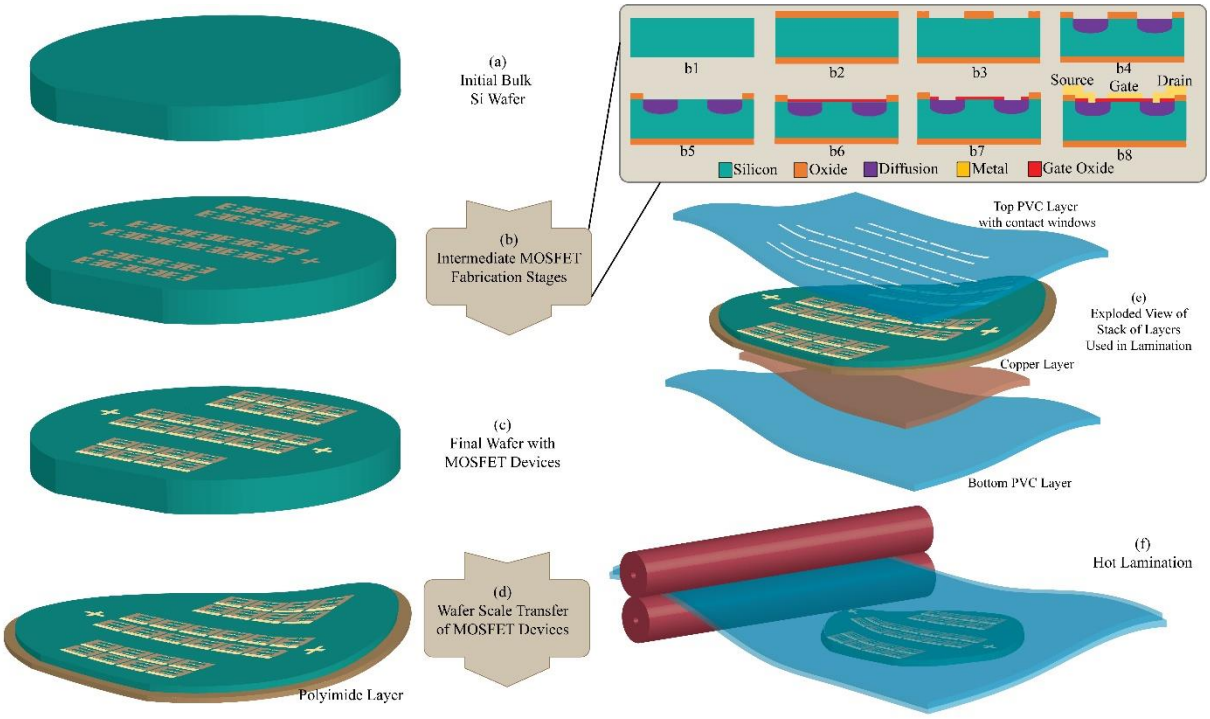


Fig. 5-2: Illustration of wafer-scale MOSFET fabrication, thinning and packaging. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

5. 2. Results and Discussion of UTC Devices

The above devices were studied in detail to gain insight into the effectiveness of proposed methodology. The effect of thinning on surface morphology and optical properties was investigated at first, which are common to all samples (**Table 13**). High-performance circuits for various application requires majorly resistors, capacitors and MOSFETs sometimes inductors and other circuit elements. To study the effect of tensile and compressive bending on response of such circuit, electrical characteristics of the resistive structures, MOS capacitor and n-MOSFET were studied. Further, many standard abstract models depending on the regions of operation consider MOSFET device as comprising of a combination of voltage controlled resistive (channel region) and capacitive components along with other parasitics. This study gives a better insight on bending induced deviations in their response[252,120,253]. Various samples used in this study are summarised in **Table 13** with their dimensions and key-findings.

5.2.1. Surface Morphology

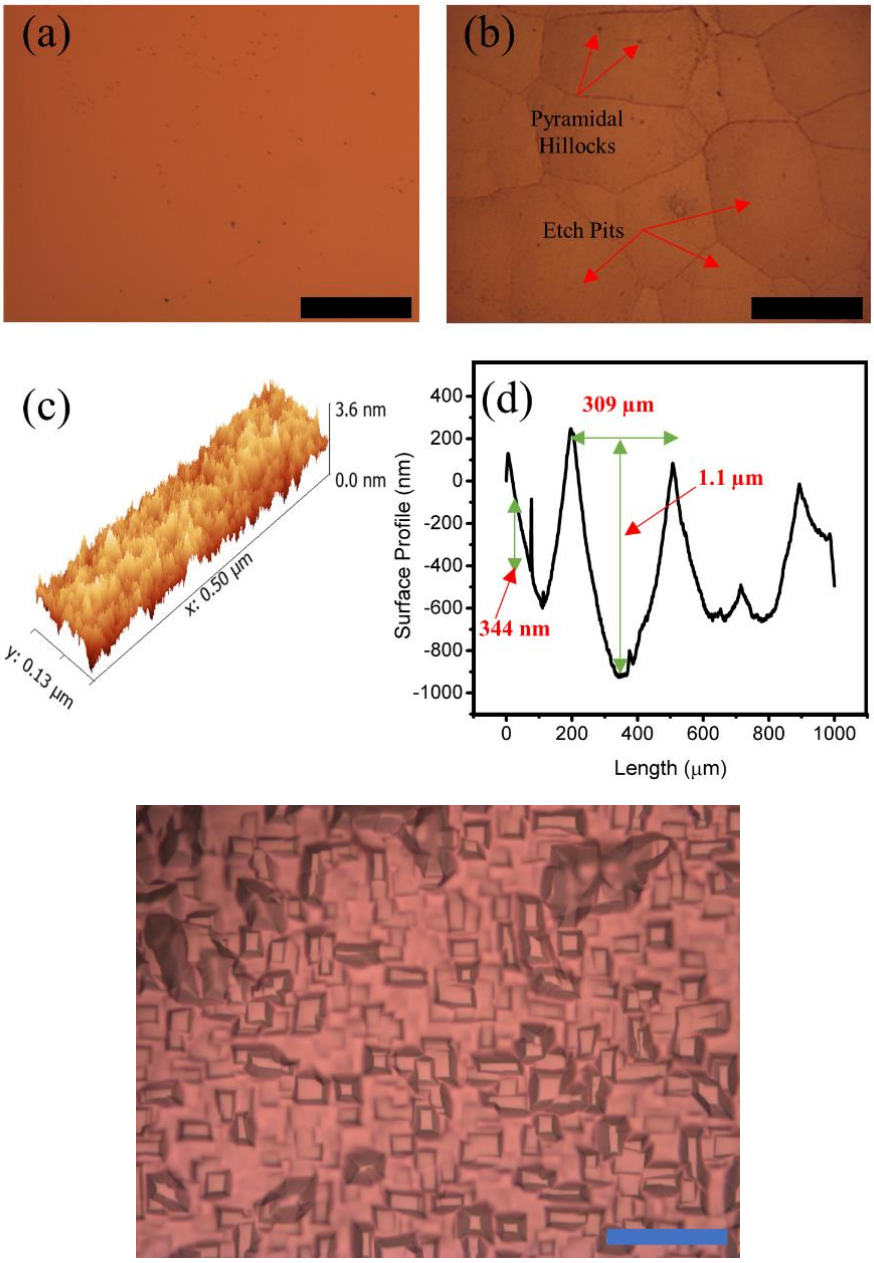


Fig. 5-3: Optical microscopic images of a) front and (Scale: 400 µm) and b) rear surface of the thinned Si (Scale: 400 µm) showing etch pits and pyramidal hillocks. c) Atomic Force Microscopy (AFM) scan of the front surface of the thinned Si showing a root-mean-square (RMS) surface roughness of 0.392 nm d) Surface profile of rear side showing etch pits (~1.1 µm deep, ~309 µm wide), pyramidal hillocks (~344 nm high) and Gaussian Filtered RMS surface roughness of 132 nm.(e) Microscopic image (100x) of Rear side of Bulk Si before thinning (Scale: 20 µm). [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim. Weinheim.

During the anisotropic wet etching, it is possible to have pyramid shape hillocks on the etched surface which leads to localised stress and can adversely affect the strength of the chip[254]. While hillocks could be reduced by adding IPA to etchant, the etch pits seem to be inherent to process. Such morphological features influence the fracture strength of Si and therefore careful selection of etchant is needed to have highest possible fracture strength along with smooth etched surface[254]. For this reason, IPA/TMAH solution was used

which is widely reported to improve the surface smoothness by increasing wettability of the TMAH etchant and decreases the formation of the hydrogen bubbles[255]. The microscopic surface morphologies of both sides of the wafer were studied. As can be seen from optical and AFM scan images in **Fig. 5-3(a)** and **Fig. 5-3(c),** the front surface is smooth with RMS surface roughness up to ~0.392 nm. However, some etch-pits and pyramidal hillocks appear on the rear surface of the sample as shown in the optical microscopic image (**Fig. 5-3(b))** and surface profilometer scan (**Fig. 5-3(d))**. Careful examination of the etched surface reveals that the surface is almost built up with circular etch pits which are ~1.1 µm deep and ~309 µm wide.

5.2.2. Optical Analysis and UV-Visible-NIR spectroscopy

Si starts to become optically transparent with decrease in the thickness, starting in the red region and progressing towards the blue region as the wafer becomes thinner. This is owing to varying absorption coefficients of Si at different wavelengths. The Fresnel equation and Beer-Lambert law explained in **section 2.2.3.3.** could be used to estimate the percentages of reflected and absorbed lights for Si thickness (>10 µm) which is not of the order of the wavelengths of the light spectrum (300 nm to 1100 nm), where interference effects are negligible.

Using the Fresnel equation, the reflectance for normal light incidence is given by:

$$\mathrm{R}\ (\%) = 100\ \left|\frac{\mathrm{n_{Air}} - \mathrm{n_{Si}(\lambda)}}{\mathrm{n_{Air}} + \mathrm{n_{Si}(\lambda)}}\right|^2 \qquad \textbf{(E 5-1)}$$

where n_{Air} is the refractive index of the air (~1.00), n_{Si} is the refractive index of Si, and λ is the optical wavelength. As per Beer-Lambert's law, the percentage of light absorbed after it passes through a given path length (x) through Si wafer is given by:

$$\mathrm{A}\ (\%) = 100\left(1 - \mathrm{e}^{-\alpha_{\mathrm{Si}}(\lambda)\mathrm{x}}\right) \qquad \textbf{(E 5-2)}$$

Where, α is the absorption coefficient of Si at a given wavelength. The optical parameters used here are based on[107].

The percentage of light transmitted without considering reflectance is given by:

$$\mathrm{T}\ (\%) = 100\ (\mathrm{e}^{-\alpha_{\mathrm{Si}}(\lambda)\mathrm{x}}) \qquad \textbf{(E 5-3)}$$

Here, the path length is equal to the thickness of Si. This assumes negligible contributions from rear reflection and diffused reflectance. The percentage of light transmitted considering reflectance only on the front side is:

$$\mathrm{T_{Net}}\ (\%) = 100\ (1 - \left|\frac{\mathrm{n_{Air}} - \mathrm{n_{Si}(\lambda)}}{\mathrm{n_{Air}} + \mathrm{n_{Si}(\lambda)}}\right|^2)(\mathrm{e}^{-\alpha_{\mathrm{Si}}(\lambda)\mathrm{t_{Si}}}) \qquad \textbf{(E 5-4)}$$

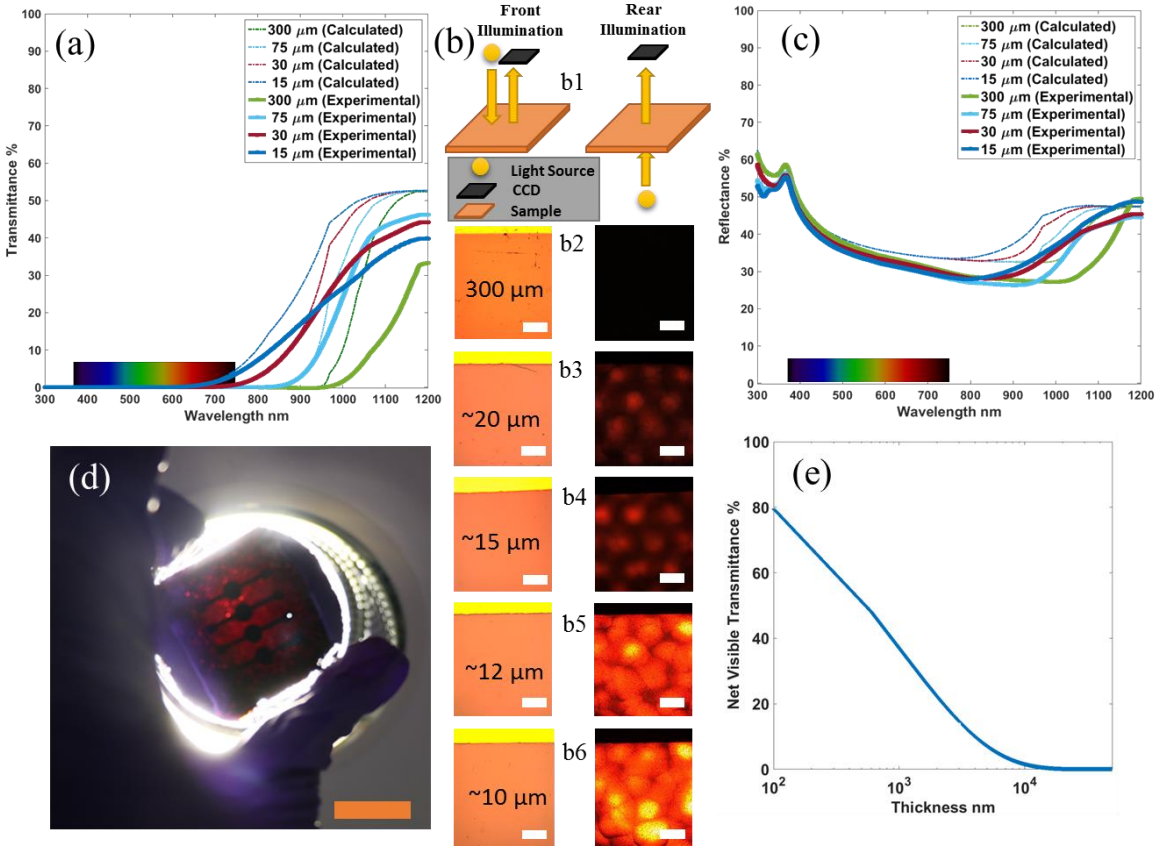


Fig. 5-4: UV-Visible-NIR a) transmittance and c) reflectance spectrum compared to the calculated spectrum for various thicknesses of Si chips b) Schematic b1) and Optical microscopic images of samples b2-b6) of different thickness imaged from front-side under front-side illumination and rear-side illumination (Scales: 300 μm). d) Thin silicon MOS capacitor structure transmitting red light under a white led light illumination (Scale: 2 cm). e) Net visible transmittance Versus Thickness of wafer. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

Fig. 5-4**(a)** and Fig. 5-4**(c)** shows the net spectral transmittance and spectral reflectance, respectively of the ultra-thin silicon samples namely UVN1, UVN2, UVN3 and UVN4, corresponding to thicknesses 15 μm, 30 μm, 75 μm and 300 μm, as given in **Table 13** (UVN stands for sample used for UV-Visible-Near-Infrared spectroscopic studies). The UV-Visible-NIR spectroscopic investigation was carried out using Shimadzu UV2600 spectrophotometer with a 60mm integrating sphere. The dashed thin lines in the figures correspond to the calculated spectral transmittance and spectral reflectance. Overall, silicon's absorption coefficient becomes lower towards red and NIR region causing an observable increase in both transmittance and reflectance (contribution from front and rear side) towards the red end of the spectrum. Since the calculations consider only specular reflectance there is a difference observed between the calculated and measured spectrum especially in the NIR and the red region. Out of the light passing through the silicon, blue and green region gets absorbed completely within 10 μm. Beyond that the absorptance decreases and reaches minimum at ~1150 nm wavelength which corresponds to the bandgap of the silicon. The photons passing through the silicon wafer gets reflected from rear end. Since the starting bulk wafer (UVN4 ~300 μm) had a saw cut and alkaline etched rear side textures (**Fig. 5-3e**) it results in higher scattering of the red and IR photons causing them to

absorb in the wafer. As the wafer is etched for long time in 25% TMAH with 10% IPA the small textures get smoothened out and shallow etch pits appear as shown in **Fig. 5-3b**. This along with thinning results in higher reflectance and transmittance in the infrared region of spectrum. The normalised net transmittance of the four samples UVN1 (~15 μm), UVN2 (~30 μm), UVN3 (~75 μm) and UVN4 (~300 μm) were 8.694%, 8.380%, 6.09% and 0.927% respectively. In the visible region UVN4 and UVN3 didn't have any observable transmittance. UVN2 and UVN1 had very low transmittances of 0.011% and 0.170% respectively. The effect is well observed in **Fig. 5-4(b2-b6)** where Si wafers of different thicknesses at various stages of thinning were illuminated as schematically shown in **Fig. 5-4(b1).** The illumination was carried out both from front side (reflection) as well as the rear side (transmission) while the image was captured always from the front side in an optical microscope**.** The top strip appearing as yellow in the top illumination and black in the bottom illumination of all the images in **Fig. 5-4(b2-b6)**) correspond to the metal used as electrode of the capacitive structure. In the sample with thickness ~300 μm, complete opaqueness is observed across the visible spectrum. However, when the thickness reaches sub-20 μm range, even though the sample looks similar in the front illumination transparency in red region starts being visible **Fig. 5-4(b3-b6).** The etch pit boundaries are also visible in the rear illumination. **Fig. 5-4(d)** shows the thinned MOSCAP wafer corresponding to **Fig. 5-8(a)** (electrical characteristics discussed later in this section) under rear illumination by a white LED light. One possible application of this behaviour could be to decide the etch completion time. Since in wet etching, the etch time plays a crucial rule and very hard to control, a red-light source could be placed at one end of etching setup and the transmittance can then be observed from other side. When the transmittance crosses the limit, which corresponds to particular thickness, etching can be stopped. This will assist in large scale manufacturing of ultra-thin chips. For application where higher absorptance is required, such as flexible silicon-based solar cells, the optical path length in thin silicon can be improved by using special optical trapping techniques such as Lambertian trapping[109,110], texturing[111], antireflection coatings[112]. **Fig. 5-4(e)** shows normalised weighted transmittance in the visible region for various thicknesses. 80% weighted visible transmittance can be achieved for Si close to 100nm thick. Such thin Si could find application to realize semi-transparent or transparent electronics. Realising this is possible using SOI technology where the oxide layer underneath could act as a supporting transparent layer for thin Si in addition to serving as an etch stop layer.

5.2.3. Effect of Bending on the devices (Resistors, MOSCAPs, MOSFETs)

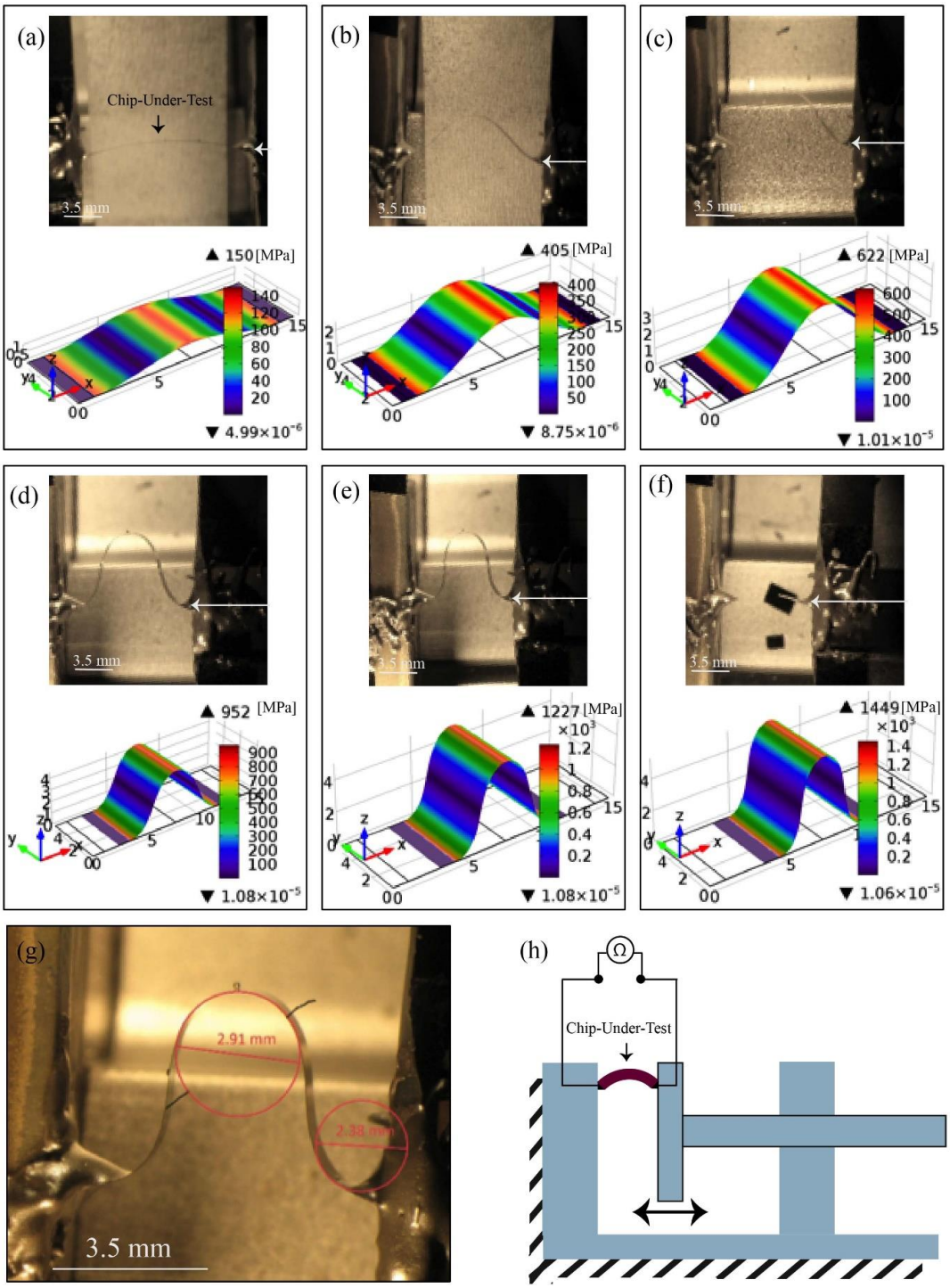


Fig. 5-5: a-f) Bending of bare Si chips (RBC2 of Table 13) anchored on both sides by silver paste together with COMSOL simulation of Von Mises Stress. g) enlarged image of Fig. 5-5(e) showing the diameter of curvature of the film implying a $R_C = 1.19$ mm at edges just before breakage (with angle correction). h) Schematic diagram of electro-mechanical bend test setup. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

It is important to examine the limits of bending and understand the stress-strain in single and multilayer electronic structures to ensure reliable operation of UTCs[118,88]. Therefore, the UTC samples were investigated by: (a) semi-analytical approach; (b) experimental

bending analysis, and (c) finite element analysis in COMSOL. For bending analysis, three types of samples i.e. RBC1, RBC2 and RBC3 were tested, as described in **Table 13**.

The samples were placed on the clamps connected to a micrometer positioning set up as illustrated in **Fig. 5-5(h)**. The sample bends as the movable end advances towards the fixed end during which images were recorded at various stages of bending as shown in **Fig. 5-5(a-f)** (for sample RBC2).

In the case of RBC1 sample, the micro-positioning jig was used to bend the membrane as shown in **Fig. 5-6**. The distance between the jigs were measured using a digital micrometer connected to the setup. The moving end was brought close to the fixed end gradually with a step size of 0.25 mm until the chip was broken. The R_{BC} extracted by curve fitting was ~1.1 mm. For a single layer Si membrane sample the theoretical value of the R_{BC}, obtained by substituting c=0, $h_0 = 0$ µm, $t_{Si} = 15.36$ µm, $y_{extreme} = t_{Si}$ is 1.097 mm in Equation **E 2-12**. This is in close agreement with the observed R_{BC}. The approximate stress at the breaking curvature of the Si chip, given by $\sigma_{BC} \approx E_{Si}\varepsilon_{BC}$ is 910 MPa.

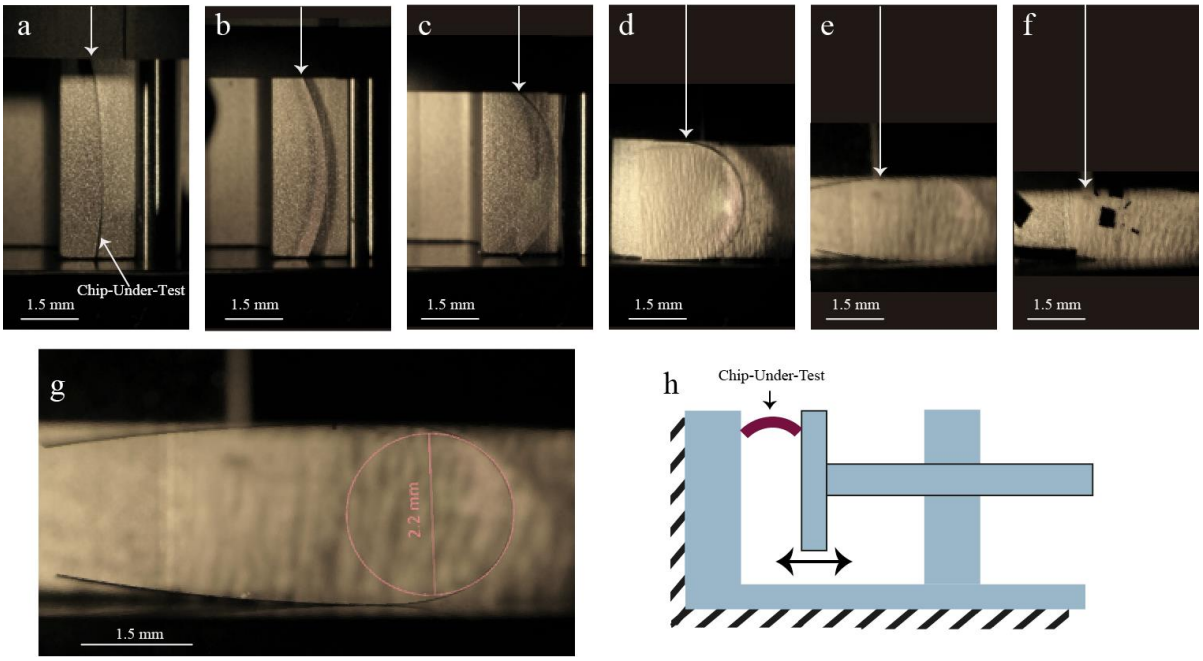


Fig. 5-6: a-f) The bending of a bare Si sample (RBC 1 of Table 13); g) the expanded view (e) showing $R_C = 1.1$ mm. h) Schematic of the bendability analysis setup. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

For RBC2 sample, the silicon membrane was anchored at both ends to the jig with conductive paste as shown in **Fig. 5-5**. The conductive paste was used for measuring electrical resistances of the sample at various bending. For this sample the R_{BC} was found to be ~1.46 mm, which is higher than the first sample. This could be attributed to the additional stresses generated because the two ends were anchored. The R_{BC} at the edges just before breakage was found to be 1.19 mm. The stress analysis was also carried out with COMSOL Multiphysics tool for various bending stages. The breaking Von-mises stress from the COMSOL simulation is ~1227 MPa, which is 30% more than the approximate analytically estimated value.

In the case of RBC3 sample i.e. Si membrane encapsulated with PI, both edges were anchored to the micro-positioning jig with conductive silver paste as shown in **Fig. 5-7**. The electrical resistances were also measured at various bent positions. In this case, the R_{BC} limit was found to be ~1.74 mm, which is more than the values for previous two samples. This could be attributed to the PI on both sides of Si and the anchoring of the two edges. The R_{BC} close to the edge just before breakage was found to be 1.475 mm. Also, it may be noted that the chip broke at the fixed point close to the right edge instead of the centre as the maximum strain occurred at this point. Theoretically, the R_{BC} was also estimated to be 1.1428 mm and 1.437 mm for concave-up and concave-down respectively and considering a multilayer stack of PI (16.48 µm) /Si (15.36 µm)/ PI (25 µm).

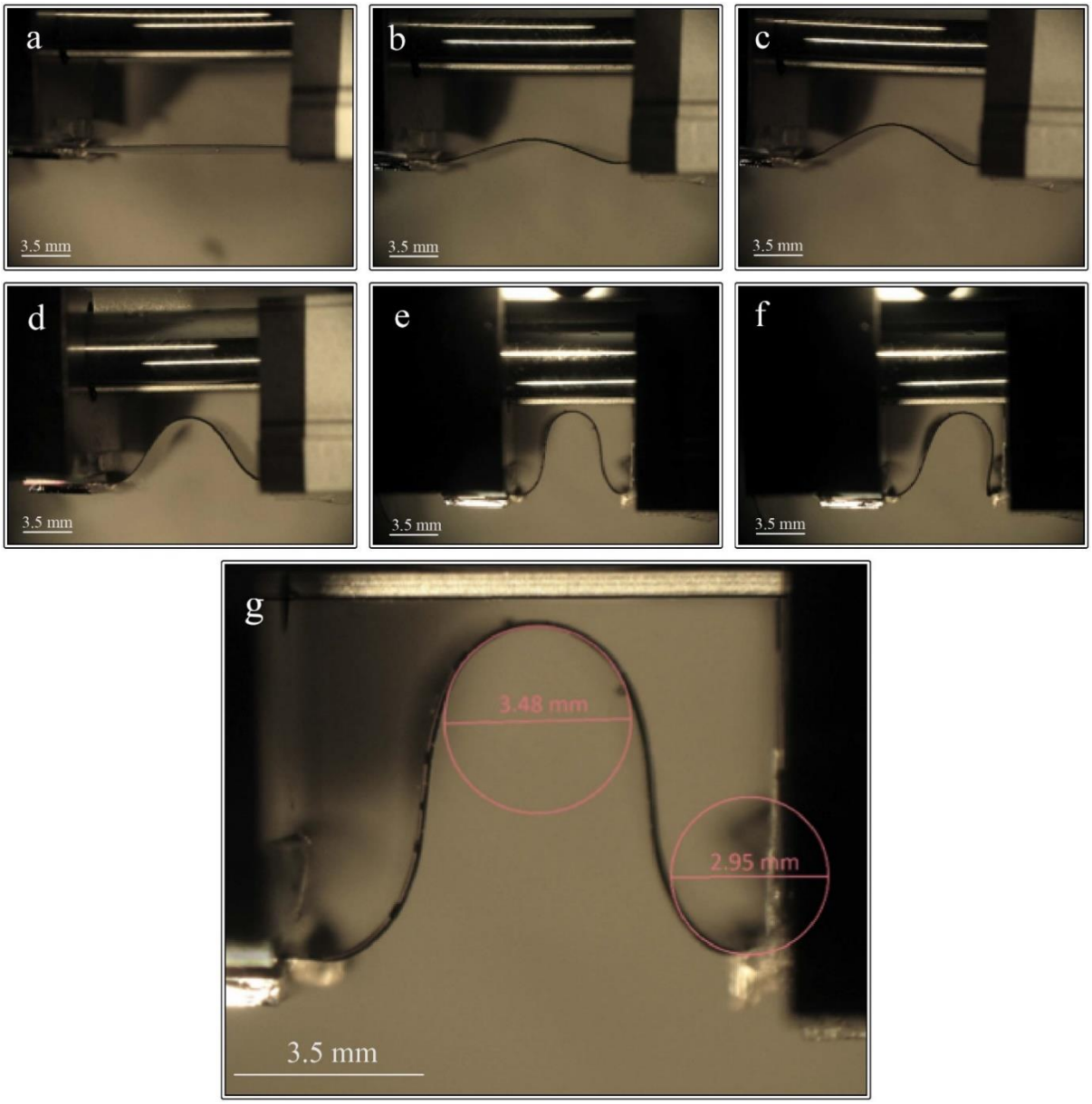


Fig. 5-7: Bending of Si chip encapsulated in PI and anchored on both sides by silver paste, (g) expanded view of Fig. 5-7(e) showing the diameter of curvature of the film implying a $R_C = 1.475$ mm just before breakage. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

These images were also used to determine the various radius of curvature, R_C by estimating the distance per pixel from the two ends of the jig and the number of pixels in the diameter formed by the circle fitting into the curved membrane with angle correction. Since the bending was carried out by anchoring the UTC between the moving and fixed jig, the top centre of the chip is under tensile stress while the top left and right edges are in compressive stress. Bottom centre of the chip is in compressive stress while the bottom left and right edges are in tensile stress. The stress varies along the thickness as well as from centre to periphery as observed in the COMSOL simulation results in **Fig. 5-5** Von Mises Stress. The distance between the two ends of the jig versus 1/Radius of Curvature at the centre is given in **Figure. S4(a**) in **Supplementary Section S4** of the published article[25]. The breaking radius of curvature, R_{BC} is the R_C just before the ultra-thin chip breaks. The experimental and theoretical values of R_{BC} are summarised in **Table 13** and its derivation is given in the **section 2.2.3.1** of **chapter 2**. The equation and the parameters used for COMSOL simulation are given in **section 3.3.1** of **chapter 3**. It may be noted that the breaking radius decreases or the structures becomes less conformable with multiple layers of materials on UTCs especially when the UTC position is shifted away from the neutral plane instead of a symmetric condition. For example, theoretical value of R_{BC} for RBC3 is ~1.475 mm, whereas the same for MOSCAP and MOSFET is ~18.897 mm.

During the bending, the electrical resistance values of the membranes (RBC2 and RBC3) were also measured using the contacts at the two ends. With UTCs bending, the top p-side (i.e. doped side) experiences a tensile strain while bottom n-side experienced a compressive strain. While the tensile strain increases the resistance of p-side, compressive strain increases the value of n-side, and since these two resistors can be in parallel, we may see an increase in combined resistance value. This results in an overall increase in the resistance of UTCs, which is mainly attributed to the piezo-resistivity. For bare Si chip (RBC2), the base resistance (i.e. corresponding to the initial zero bending state) was found to be 17.27 kΩ and a maximum increase of 3.8% was observed just before the breaking radius of curvature (**Figure. S4-(b)** [25]). In case of polyimide (PI)/Si/PI (RBC3), the base resistance was 6.21 kΩ with a maximum percentage increase of 1.2%. This neglects the region closer to the breaking radius of curvature where the resistance went up to >14.2 kΩ as can be seen from **Figure. S4-(c)** [25]. The sudden increase in resistance could be attributed to microcracks possibly developed at the contacts but the polyimide keeping the structure together.

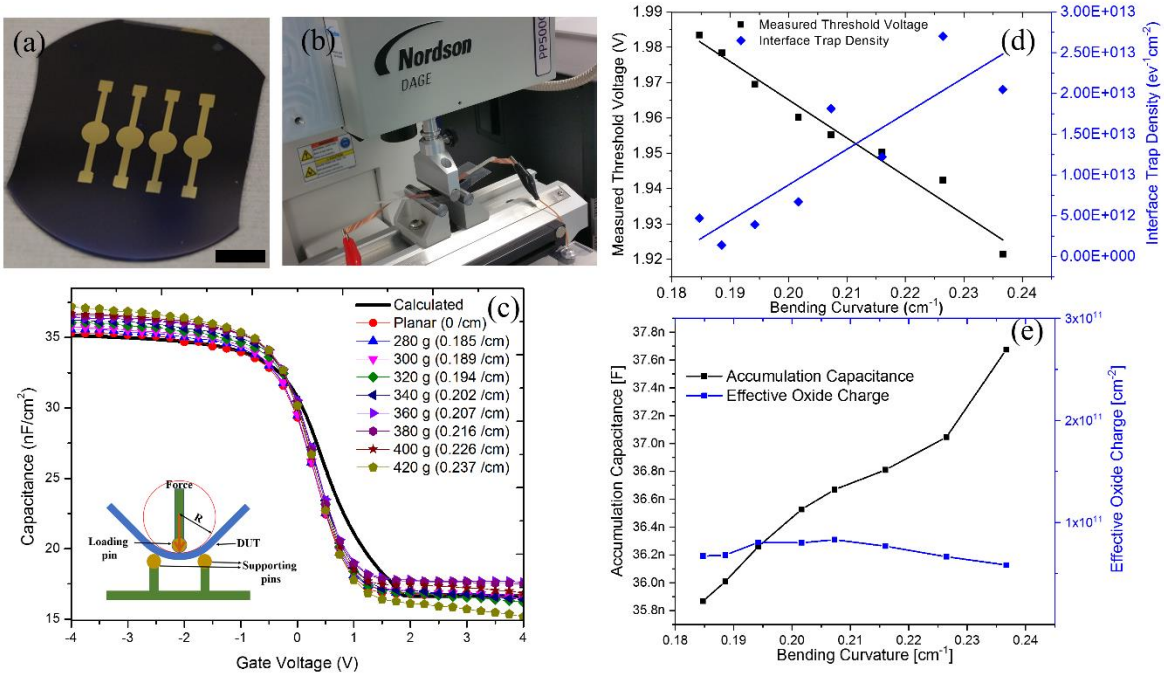


Fig. 5-8: a) Image of fabricated MOSCAPs (scale: 1 cm). b) Device Under Test (DUT) using 3-point bending setup. c) C-V characteristics under ideal and various bending conditions. d) Bending curvature Vs threshold voltage and interface trap density. e) Bending curvature Vs accumulation capacitance and effective oxide charge. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

MOS capacitor is an essential part of a MOSFET. So, to study the effect of bending on MOSFET, it is necessary to study how various parameters change during the bending of MOS capacitor. The MOSCAP was evaluated for bending by using a Nordson Dage 3-point bending set up (**Fig. 5-8(b)**) as explained in **section 3.2.7.1**. The samples were encapsulated in poly(vinyl chloride) (PVC) sheets using hot lamination method and then various loading forces and corresponding displacements were measured. The C-V measurements of the MOSCAP device under planar and various bending conditions (**Fig. 5-8(c)**) were made with a semiconductor parameter analyser at 1MHz frequency. The C-V sweep was carried out with DC voltage from -4 to 4 Volts superimposed with a 50 mV AC voltage. Change in the CV characteristics was observed with bending and up to 5% increase in capacitance was measured at bending radius of 42 mm. The bending radius of curvature was calculated from the vertical displacement assuming the membrane width as arc length and displacement as chord of a circle. The ideal CV characteristics calculated with MATLAB code with given doping and oxide thickness corresponding to accumulation capacitance is also shown in **Fig. 5-8(c)** and derivation of ideal CV is provided in **section 3.2.6.1** of **chapter 3**). The measured CV characteristics differ from the calculated value due to the presence of various charges in the oxide (namely, fixed oxide charges, mobile ionic charges, interface trapped charges), work function of the metal, interface trap density as well as the effect of bending on doping and other parameters. It may be noted from **Fig. 5-8(d)** that the interface trap density increases and the V_{th} decreases as the bending curvature increases. In addition, an increase in accumulation capacitance value upon increasing tensile strain was observed and plotted in **Fig. 5-8(e).** Also, it is worthy to note that the effective oxide charge value remained almost constant during bending. The variation in threshold voltage upon bending, can change the operating point of device and so proper compensation circuit might be needed. Various

device and interface parameters extracted by comparing the measured and ideal CV characteristic are summarised in **Table 14**.

Table 14: Various MOSCAP parameters calculated from C-V characteristics obtained from planar condition

MOSCAP Parameters in planar condition	Value
Threshold voltage	1.99319 V
Effective oxide charge	6.88×10^{10} /cm^2
Interface trap density	8.65×10^{11} /cm^2-eV
Depletion width	327 nm
Flatband capacitance	31.1 nF
Flatband voltage	-0.189 V
Accumulation capacitance	35.6 nF/cm^2

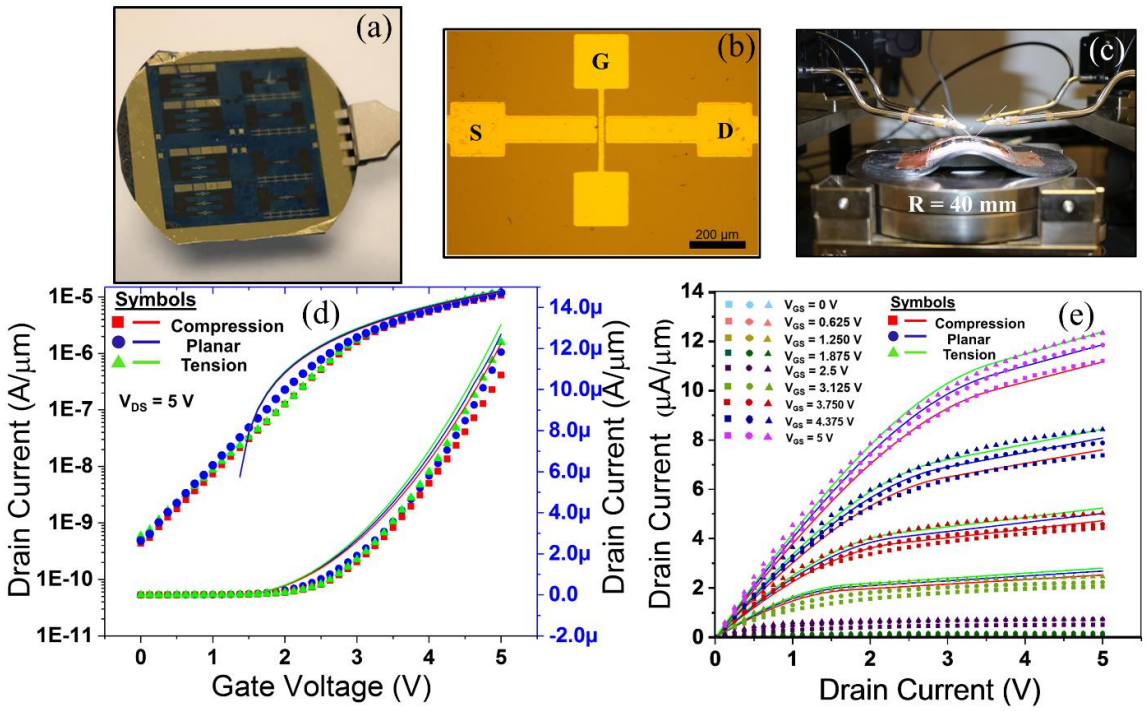


Fig. 5-9: a) Si wafer with MOSFETs. b) Optical image of single MOSFET (W = 100 µm, L=10 µm). c) Arrangement for electrical characterisation under bending conditions. The MOSFETs are placed on 3D printed curved surfaces of different curvatures. The MOSFETs are placed on 3D printed curved surfaces of different curvatures. d) Transfer characteristic of MOSFET [experimental (dots) Vs simulation (line)] under planar (blue line), compressive (red line) and tensile (green line) bending condition. e) Output characteristic of MOSFET [experimental (dots) Vs simulation (line)] under planar (blue line), compressive (red line) and tensile (green line) bending condition. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

The fabricated MOSFET devices on wafer-scale is shown in **Fig. 5-9(a).** The microscopic image of single MOSFET is shown in **Fig. 5-9(b).** After thinning and transfer printing as described before, the MOSFETs devices were evaluated under various bending conditions. To observe the effect of bending stress, the laminated thinned wafer was placed on 3D printed convex and concave structures (R = 40 mm) as shown in **Fig. 5-9(c)** and

explained in **section 3.2.7.1**. In convex bending, the devices come under tensile stress whereas they experience compressive stress in the case of concave bending. The strain generated due to mechanical bending is known to affect the band structure of material[102]. As presented in section 2.2.3.4, formulated analytical equations relating the stress with the mobility and drain current[119,118] is given as:

$$\mu_{(\text{stress})} = \mu_o\left(1 \pm \Pi_\mu \sigma_\mu\right) \quad \textbf{(E 5-5)}$$

$$I_{D(\text{stress})} = I_{D_0}\left(1 \pm \Pi_{I_D} \sigma_{I_D}\right) \quad \textbf{(E5-6)}$$

where μ_0, I_{D0}, μ_{stress} and $I_{Dstress}$ are mobility and drain current under normal and stressed conditions respectively. The piezoresistive coefficients Π_μ and Π_{ID} accounts for sensitivity towards stress and σ is magnitude of stress[120]. In n-MOSFET, the channel is n-type where the resistance decreases and gate oxide capacitance increases with tensile bending. This means the tensile strain leads to overall increase in the current and opposite happens for compressive strain. This is indicated by the transfer and output characteristics of transistor in **Fig. 5-9(d)** and **Fig. 5-9(e)** respectively. These characteristics were obtained under different bending conditions. Various parameters extracted from the electrical characterisation of the MOSFET under planar and bending conditions are summarised in Table 15. The effective surface mobility μ_{eff} was calculated by the equation:

$$\mu_{eff} = \frac{L}{W}\frac{g_d}{C_{ox}(V_{GS}-V_{th})} \quad \textbf{(E 5-7)}$$

Table 15: Various parameters related to MOSFET characteristics

Parameters	**Tensile Strain**	**Planar**	**Compressive Strain**
Bending Radius of Curvature R_C	40 mm (Convex)	-	40 mm (Concave)
Effective Mobility (Experimental) μ_{eff}	384 cm^2/V-s	350 cm^2/V-s	333 cm^2/V-s
Saturation Mobility (Experimental) μ_{sat}	355 cm^2/V-s	341 cm^2/V-s	320 cm^2/V-s
Saturation Mobility (Semi-empirical) $\mu_{sat\text{-}Cal}$	353 cm^2/V-s	341 cm^2/V-s (Ref.)	327 cm^2/V-s
Threshold voltage (V_{th})	1.305 V	1.425 V	1.55 V
Channel-length Modulation Factor (λ)	0.094	0.115	0.122
Saturation Current ($I_{D\text{-}sat}$) at V_{DS}=5 and V_{GS}=5V	12.3 µA/µm	11.8 µA/µm	10.7 µA/µm
Drain Conductance (g_d)	4.94 µS/µm	4.58 µS/µm	4.06 µS/µm
I_{ON}/I_{OFF}	4.32 decades (2.08×10^4)	4.38 decades (2.42×10^4)	4.39 decades (2.46×10^4)
SS	1.06 V/decade	0.98 V/decade	1.04 V/decade
Transconductance (g_m)	6.67 µS/µm	6.62 µS/µm	6.21 µS/µm
Gate Delay	0.23 ns	0.27 ns	0.3 ns

Where L and W are the length and width of the MOSFET, g_d is the drain conductance, C_{ox} is the oxide capacitance and V_{th} is the threshold voltage. The threshold voltage (extracted from linear extrapolation method[234]) under tensile bending, planar and compressive

bending conditions are 1.305, 1.425 and 1.55 V, respectively. The drain conductance is given by the equation:

$$g_d = \frac{\partial I_D}{\partial V_{DS}} | V_{GS} = Constant \quad \textbf{(E 5-8)}$$

The drain conductances at tensile, planar and compressive conditions were estimated from the V_{DS}-I_D characteristics by numerically differentiating the drain current with reference to the drain-source voltage and their values were 4.94, 4.58 and 4.06 µS/µm respectively. The maximum transconductance of the n-MOSFET under planar and bending conditions were calculated as per the equation by numerically differentiating the values in Matlab:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} | V_{DS} = Constant \quad \textbf{(E 5-9)}$$

The estimated effective surface mobility for the three conditions were 384, 350 and 333 cm^2/V-s, respectively.

For theoretical calculation of change in mobility, the stack was considered to be composed of five layers, PVC, copper, PI, Si and PVC from bottom to top respectively. The values of Young's modulus and thicknesses used for this calculation are given in **Table 16**. Strain experienced by silicon layer is calculated using Equations (**E 2-8**) to (**E 2-9**) and multiplied by Young's Modulus of silicon to get stress value. For tensile bending strain ($\varepsilon_{tensile}$) is calculated to be 0.819 x 10^{-3} and for compressive bending strain (ε_{comp}) it is -0.805 x 10^{-3}. The difference in $\varepsilon_{tensile}$ and ε_{comp} is because of the asymmetric package design, as silicon is fourth layer from bottom but second layer from top. The net piezoresistive coefficient (Π_μ) can be written as function of piezoresistive coefficients of FET[102]:

$$\Pi_\mu = \frac{(\Pi_{11} + \Pi_{12} + \Pi_{44})}{2} \quad \textbf{(E 5-10)}$$

and the value is calculated to be 311x10^{-12} Pa^{-1}.

Table 16: Young's modulus and thickness of materials used for strain calculation

Material	Young's Modulus (GPa)	Thickness (µm)
PVC	3	100
PI	2.5	15
Copper	120	50
Si	150	15

Using the value of Π_μ, $\varepsilon_{tensile}$, ε_{comp} and μ_o, the theoretical value of mobilities under tensile and compressive bending are 353 cm^2/V-s and 328 cm^2/V-s.

Table 17: Theoretical values of strain, stress and mobility under tensile and compressive bending condition

Parameter	Tensile	Compressive
Strain	0.819 x 10^{-3}	-0.805 x 10^{-3}
Stress	122.85 MPa	120.75 MPa
Mobility	353 cm^2/V-s	328 cm^2/V-s

The key theoretical values are tabulated in **Table 17**, and as can be seen that the calculated mobility values are very close to the experimental values.

The saturation mobility (μ_{sat}) obtained from output characteristic under planar condition is 341 *cm^2/V-s*. However, with convex and concave bending, the mobility (with same biasing conditions) was found to be 355 *cm^2/V-s* and 320 *cm^2/V-s* respectively. Using Equations. **(E 5-5)** and **(E5-6)**, the semi-empirically (in relation to planar saturation mobility) estimated value of mobilities under tensile (convex) and compressive (concave) bending are 353 *cm^2/V-s* and 327 *cm^2/V-s*. Thus, semi-empirical values closely match and deviate only by 0.5% and 2.5% from the experimentally obtained mobility values.

The change in current level can be primarily attributed to change in oxide capacitance, interface effects and mobility. Since, current is directly proportional to both capacitance and mobility, for small change, it can be written as:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta C_{ox}}{C_{ox}} + \frac{\Delta \mu}{\mu} \qquad \textbf{(E 5-11)}$$

At R = 40 mm, the theoretical change in mobility and capacitance are around 3.82% and 5% respectively, which lead to about 8% change in the current. This also matches with experimental measurements, which show a maximum of ~10% change in the current. The saturation current (at V_{DS}=*5V* and V_{GS}=5V) were 12.3, 11.8, 10.7 μA/μm for tensile, planar and compressive conditions respectively. The on-to-off current ratios for the three cases were 4.32, 4.38 and 4.39 decades. Subthreshold slope (SS) was estimated from the logarithmic transfer characteristics at subthreshold regime by numerical differentiation and is given by the equation:

$$SS = \frac{1}{\partial \log(I_D)/\partial V_{GS}} \qquad \textbf{(E 5-12)}$$

The subthreshold slope for tensile, planar and compressive conditions were 1.06, 0.98 and 1.04 V/decade. The SS values are higher because the device was a planar, long channel MOSFET, with ~100 nm SiO_2 as dielectric. By realising, advanced FET structures such as FinFET and by using High-K dielectric better subthreshold voltage can be achieved[245]. The approximate gate delay for a typical CMOS application assuming a fanout (f_n) of 2 and symmetric balanced CMOS (i.e. μ_{eff}, L and W of n-MOS and p-MOSFET) was indirectly calculated from the below equation[253]:

$$\tau_{GD} = \frac{12\, f_n}{\mu_{eff}} L_{Min}^2 \frac{V_{DD}}{(V_{DD}-V_{th})^2} \qquad \textbf{(E 5-13)}$$

The calculated gate delays were 0.23, 0.27 and 0.3 ns for tensile, planar and compressive conditions which implies ~3 GHz operation with a variation of ~11 to 15%. The changes in device response with bending has a bearing on the performance of circuits. Evaluation of device response under various bending conditions will help electronic designers to consider such variations in their design – either to negate such effects or to take advantage of such effects as sensors. Moreover, by further thinning (for e.g. using Chemical Mechanical Polishing) and optimal packaging in material of less Young's modulus and in the neutral plane the stress variation can be reduced significantly.

In order to evaluate the effect of cyclic bending on device performance, we characterised the MOSFET in planar condition after every 10 cycles of compressive and tensile bending over 3D printed zig of R_C 80 mm. A total of 100 bending cycles were carried out. Gate leakage current density (J_G) characteristics were also obtained during initial planar condition

and after 50th and 100th cycle. The plots of MOSFET transfer characteristics and leakage current densities are shown in Fig. 5-10(a) and Fig. 5-10(b) respectively. Statistically the device performance remains unaffected even after 100 bending cycles with an inter quartile range variation of less than 1.1% in I_{DSAT} and negligible variation in the leakage current density when the gate voltage is positive. In order to evaluate the device-to-device variability four MOSFETs were characterised at various locations and the results are shown in in Fig. 5-10(c). The device characteristics of three out of four devices were uniform with a variation of 3% in the I_{DSAT}.

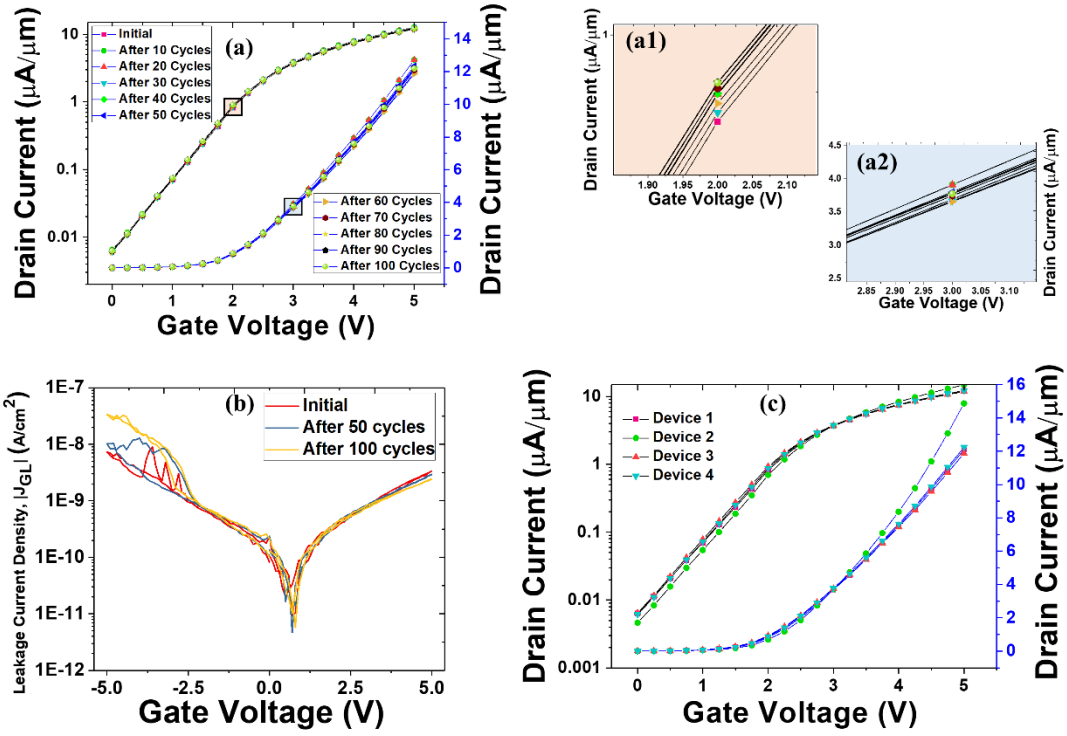


Fig. 5-10: a) Transfer characteristic of MOSFET under cyclic bending test. b) Leakage current density of MOSFET at Initial condition, mid and end of cyclic bending test. c) Device-to-device variation in transfer characteristics for four MOSFETs. [25]© 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

The changes in device response with bending has a bearing on the performance of circuits and evaluation of devices response under various bending conditions will help electronic designers to consider such variations in their design – either to negate such effects or to take advantage (for example, improving device performance by introducing stresses or using stress map to predict the shape of ultra-thin chip or the surface on which the chips are integrated). Moreover, by further thinning (for e.g. using Chemical Mechanical Polishing) and optimal packaging in material of less young's modulus and in the neutral plane the stress variation can be reduced significantly.

5. 3. Application of UTCs to realize Active Tactile Sensors

Passive tactile sensing structures can be interfaced with MOSFETs to realize active tactile elements. The capacitive static sensor and the piezoelectric dynamic sensing structure discussed in **chapter 4** are attached in an extended configuration to a fabricated MOSFET present in **section 5. 2.** to realize an active tactile sensor. The results are presented in this section. This acts as a step towards utilising UTCs for e-skin. As presented in **section 2.4.3**, there are several advantages in the marriage of sensing structure and the MOSFET such as

event driven signalling, better integration, better signal-to-noise-ratio, faster response, wider bandwidth, better force sensitivity, and no interconnect is required between transducer and electronic devices [206,41]. Further, such transistor could form directly a component of an amplifier or a higher order circuit [119].

The schema in which these sensors are connected are shown in Fig. 5-11.

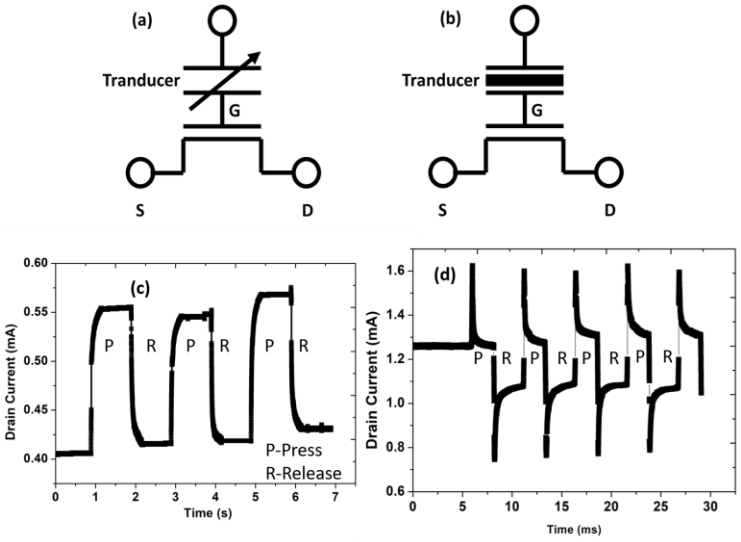


Fig. 5-11: MOSFET based extended gate (a) capacitive pressure sensor (b) piezoelectric pressure sensor (c & d) their transient response respectively for 400 kPa pulse force.

Capacitive and piezoelectric transducer was connected in extended gate mode as depicted in **Fig. 5-11a** and **Fig. 5-11b** and was tested by the setup explained in **sections 3.2.8.1**. The transistor was able to convert the change in the capacitance and the change in the piezoelectric charge to voltage as seen in the **Fig. 5-11c&d**.

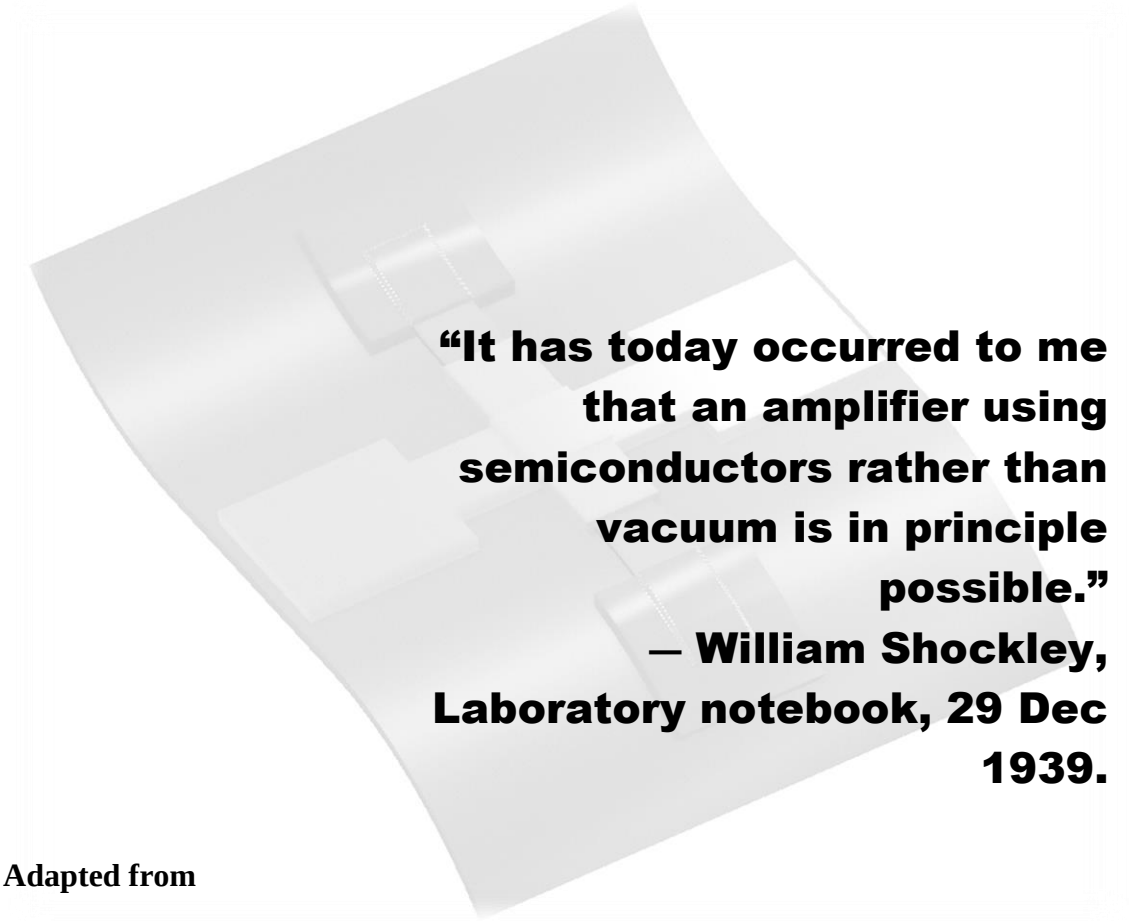
5. 4. Summary

The high-performance requirement for various flexible electronics applications can be met with Si based electronics, if ways can be found to overcome the rigidness and brittle nature of Si. In this direction, the approach for wafer-scale transfer of UTCs on flexible substrates presented in this paper is promising. Such scalable routes are required for realizing active sensors (by combining with passive sensors) and as addressing/processing elements for e-skin. The methodology has been used to obtain Si chips (~15 μm thick) with various devices including resistors, MOSCAP and MOSFETs on polyimide substrate and they have been analysed for critical bending, surface micro-morphology and the change in optical properties. The optical study carried out through UV-Visible-NIR, shows that as the thickness of Si decreases, the transparency increases in the red region. This property could be used to control the etching or for new applications such as detectors where certain degree of transparency is needed close to red region. Chemical thinning of bulk silicon chips may not be an effective strategy for achieving transparent silicon due to the etch pit and hillocks formation. For this, a combination of anisotropic etching (to realize ~15 μm silicon) and subsequent chemical mechanical polishing could be helpful. The changes in the response of MOSFETs during electro-mechanical characterisation closely match with the theoretical calculations, which allows modelling the behaviour of these devices with conventional CAD tools. This will open new opportunity for designing circuits on flexible substrate and

evaluation of their performance. For a typical device, the estimated effective surface mobility for tensile, planar and compressive bending conditions were 384, 350 and 333 cm2/V-s, respectively. While there is still scope for improvement of the performance parameters, the results are suitable for using it as a high-performance element for flexible electronics particularly in e-skin. Overall, the work demonstrates the efficacy of the new methodology presented here for wafer scale transfer of ultrathin chips on flexible substrates.

6

Nano-ribbons



“It has today occurred to me that an amplifier using semiconductors rather than vacuum is in principle possible.”
— William Shockley, Laboratory notebook, 29 Dec 1939.

Adapted from

W. T. Navaraj, N. Yogeswaran, V. Vinciguerra and R. Dahiya, *Simulation Study of Junctionless Silicon Nanoribbon FETs for High-Performance Printable Electronics,* IEEE-ECCTD, 2017, Copyright © 2017, IEEE.

Contents

6. Nano-ribbons

Controlled doping at defined locations is critical to obtain transistors which are fundamental component for flexible electronics. Achieving doping is difficult once these structures are transferred to flexible substrates owing to thermal budget issues. Without heavy doping in source and drain, it is not possible to achieve ohmic contact. There are some attempts to address this issue through alternative means such as using Si/Ge heterostructures [256]. However, CMOS circuitry is not achievable with this approach as they lead to only p-MOS devices. This highlights the need to further explore alternative solutions. The junctionless FETs (JLFET) or gated resistors reported recently is a potential route for realising CMOS circuits as in this case entire micro/nanostructures could be doped before these structures are transferred or printed on to flexible substrates [257]. Additionally, the issue related to precise registration/printing of source drain contacts at defined location also can be addressed by this approach.

This chapter is organised as follows. The structure of the nanoribbon based JLFET is presented in the section 6. 1. This section also explains the difference of device presented here with respect to the conventional nanowire based JLFETs. This is followed by discussion related to simulation results in Section 6. 2. The Technology Computer Aided Design (TCAD) based simulation is used to optimize the device. The simulation highlights why the gate is required to surround the nanoribbon. The effect of doping, thickness, workfunction etc. on the performance of the nanoribbon based JLFET are also presented in Section 6. 2. Further, section 6. 3. presents the fabrication process of the NR based JLFET followed by results and discussion. Finally, the key results are summarised in the concluding Section 6. 5.

6. 1. Structure and Operation of NR-JLFET

The operation of conventional transistors relies on the presence of p-n junction at the source/drain and formation or depletion of the channel region based on the applied bias, which determines the flow of current. Realising precisely-controlled source/drain doping on nanostructures, transfer printing and then subsequent precise registration/printing of source drain contacts over these nanostructures on flexible substrates is a major challenge for large scale production. To achieve this, the alignment patterns also should be of the same precision compared to the p-n junction within the active structures. Recently, junctionless field effect transistors (JLFET) also referred to as gated resistors that have uniform doping profile from source to the drain end of the device have been proposed to address problems in CMOS scaling[257]. Using junctionless technology on flexible electronics will eliminate the need for precise registration requirement over the doped regions.

The two prerequisites for JLFETs are: (1) Thin semiconductor layer to enable full depletion of the channel in its off state; and (2) Highly doped semiconductor to allow for realistic current drive in its ON-state as well as provide ohmic source and drain contacts [257,258]. In addition, normally off operation is required for JLFETs to be used in conventional CMOS applications. In the conventional junctionless nanowire FET, polysilicon gate of opposite polarity has been used for achieving normally off transistor. To achieve the normally off condition, n^+ polysilicon is used as the gate material for p+ channel (or p^+ polysilicon gate for n+ channel) in the originally reported junctionless nanowire FETs [258-260]. The JLFETs we propose in this work meets the above conditions, but instead of using nanowires, we have used nanoribbons as this allows devices with higher ON current. The higher channel width in nanoribbons allows higher current in comparison with

nanowires based JLFETs. Deposition of polysilicon needs high temperature and add to the thermal budget which is not possible on flexible substrates. In this regard, exploiting the metal gate work function to achieve enhancement mode transistor is promising. Further, the metal gate can be deposited at low temperature or even printed, which is critical for flexible electronics applications.

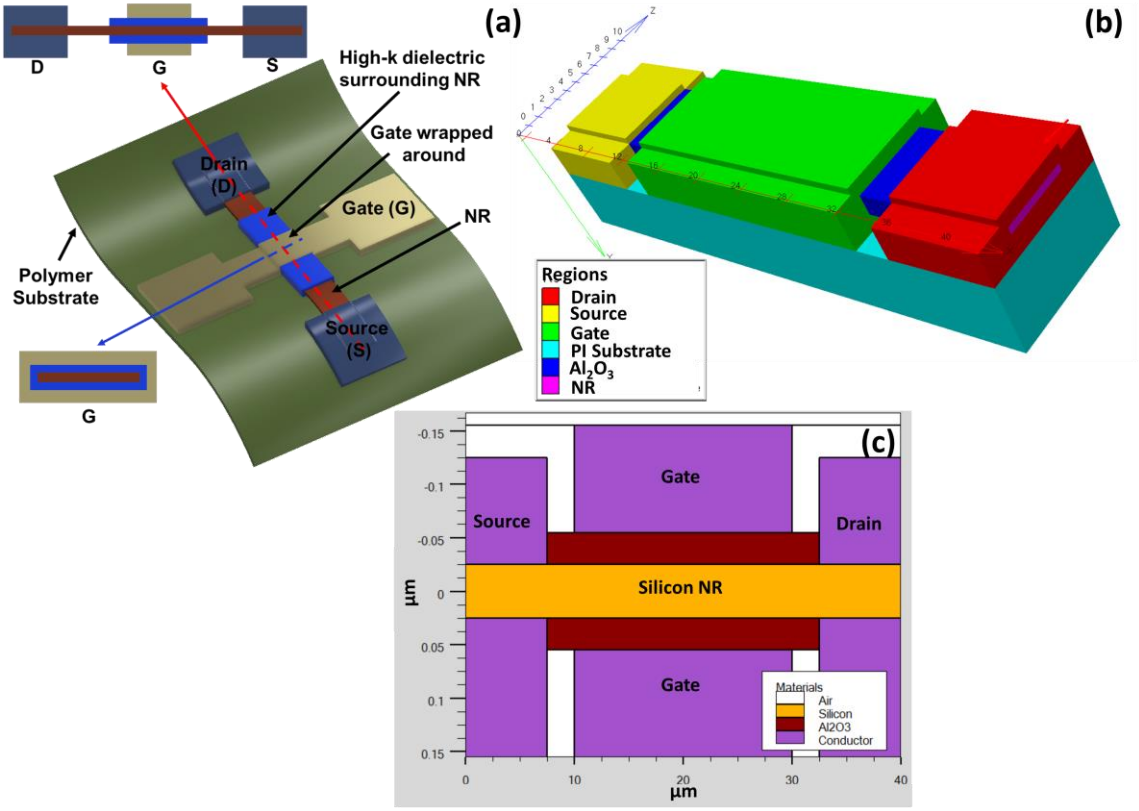


Fig. 6-1: (a) 3D schematic illustration of the Si nanoribbon based JLFET and the corresponding cross-sectional illustrations at two different cutline directions. Snapshots of the (b) 3D simulation structure and its equivalent (c) 2D simulation structure with the two gate electrode considered to be electrically a single electrical node.

Fig. 6-1(a) shows the 3D illustration of the nanoribbon based JLFET on a flexible polymer substrate and the corresponding cross-sectional illustrations at two different cutline directions. The structure of the device presented here has been designed considering that the transfer-printing based processing technology presented later will be used to realize them on flexible substrates such as polyimide. A silicon nanoribbon forms the active material with uniform heavy doping throughout the structure. A high-k dielectric wraps around the nanoribbon on the channel region. Over the dielectric, a gate metal wraps around the nanoribbon. The source and drain metal forms contact with the nanoribbon on the either side. Owing to the heavy doping, it forms ohmic contact in the source drain region. The transistor works like a gated resistor i.e. the resistance changes as per the effective gate voltage. Initially both 3D and 2D simulation of the structure was carried out. The snapshot of the simulation structure (from the simulation tool ATLAS) of 3D structure and its equivalent 2D structure corresponding to the lateral cross-section (red cutline) are shown in Fig. 6-1(b) and Fig. 6-1(c) respectively. The 2D structure was simulated so as to compare the accuracy with the 3D simulation as the latter often requires intensive computing and longer time to converge. The horizontal and the vertical axis in Fig. 6-1(c) are not of same scale. The initial

simulated device considered 50-nm thick Si nanoribbon. An initial uniform doping concentration of $1x10^{18}$ cm^{-3} is considered throughout the nanoribbon without any junction. In subsequent simulation, this doping concentration was varied. A metal gate forming a channel length of 20 µm with a work function of 5.15 eV (corresponding to Ni) is used to realize a gate all-around transistor structure. Considering the channel length is in micron scale to suit printable flexible electronics is also a differentiating factor compared to the conventional nanowires based JLFET where the channel length is in nanoscale [258]. In the case of 2D, the top and bottom gate is considered as a forming a single node gate in the simulation. A common mode gate voltage is applied during simulation to mimic the wrapped gate, around the nanoribbon. The metal gate is isolated from the active region of the device by a 30-nm thick Al_2O_3 ($\kappa\sim 9.3$) dielectric wrapping around the nanoribbon. In the case of 2D, commonly connected top and bottom gates are considered. This resembles a double gate structure. A gap of 2.5 µm was considered between source and the gate region. The models used for the simulation studies include concentration dependent mobility, field dependent mobility, Fermi-Dirac statistics, auger recombination, quantum effects[236]. The results are summarised in the next section.

6. 2. Simulation Results

Simulation studies of the device behavior is needed to cost-effectively analyze various structure and the effects of electrical parameters on device performance before fabrication. The effect of single Vs. double gate (2D equivalent), nanoribbon thickness, doping etc. are presented in this chapter. The simulations were carried out with Silvaco ATLAS 3D and 2D packages [236]. The simulations were primarily carried out for n-channel nanoribbon-based JLFET.

6.2.1. 3D Vs 2D Simulation of JLFET

A comparative study was carried out to evaluate the difference between the results from 2D and 3D structures and whether 2D simulation is sufficient. For 2D simulation, a common gate voltage was applied to both the top and bottom gate terminal considered as a single node. The drain current from both the simulations were normalised to unit channel width. The results of the 2D and 3D structure simulations are shown in Fig. 6-2. A difference of <2.2% was observed between the transfer characteristics of the 3D and 2D simulation at 1.5 V. The difference is attributed to the field effect at the edges of the nanoribbon which can be safely neglected for this study. The rest of the simulation study presented in this chapter is based on the 2D structure.

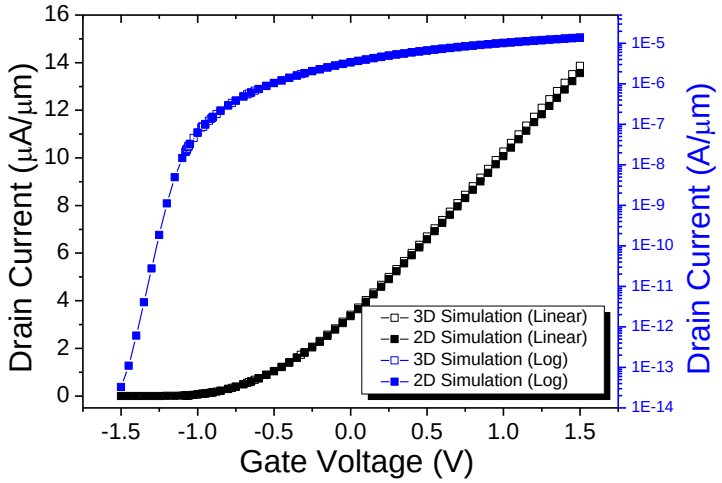
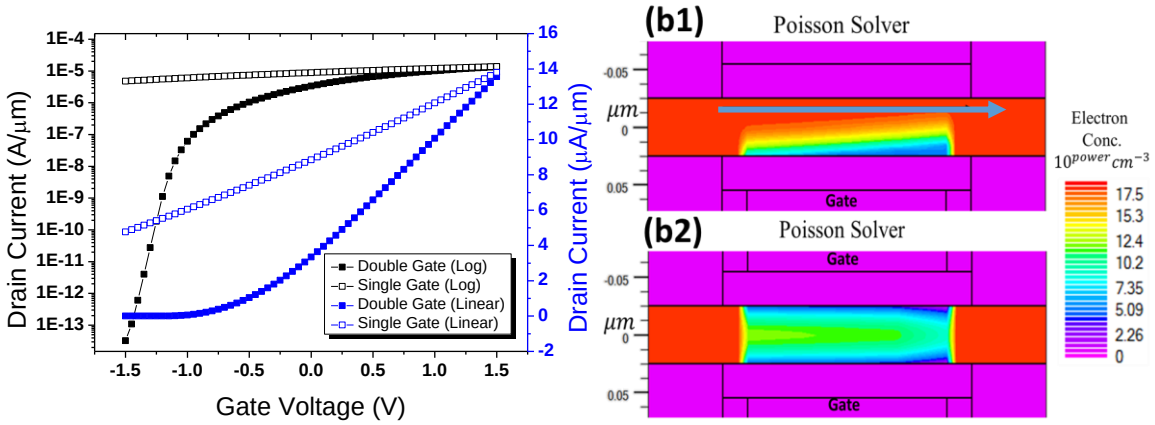


Fig. 6-2: Comparison between 3D and 2D simulation of V_{GS} Vs I_{DS} Characteristics at V_{DS}=1.5 V

6.2.2. Effect of Single Gate and Double Gate

Fig. 6-3 shows the effect of single gate and common mode double gate on the transfer characteristics of the JLFET. A single gated JLFET results in a leaky resistive channel with poor gate control as the gate is incapable of completely depleting the highly doped nanoribbon channel of JLFET. This is evident from the electron concentration contour plot shown in Fig. 6-3(b1) at V_{GS}=-1.5V compared to Fig. 6-3(b2). With a single gate, the channel is not depleted effectively and a low resistivity leaky path is observed far from the single gate as indicated by the arrow mark. Double gate results in better I-V characteristics with $\frac{I_{D+}(V_{GS}=+1.5\text{V})}{I_{D-}(V_{GS}=-1.5\text{V})}$ of 4.2x10^8, which is seven orders of magnitude higher compared to the single gate where it was mere 2.9. This shows that having a double gate is critical for JLFET and key to achieve a higher on-to-off ratio.



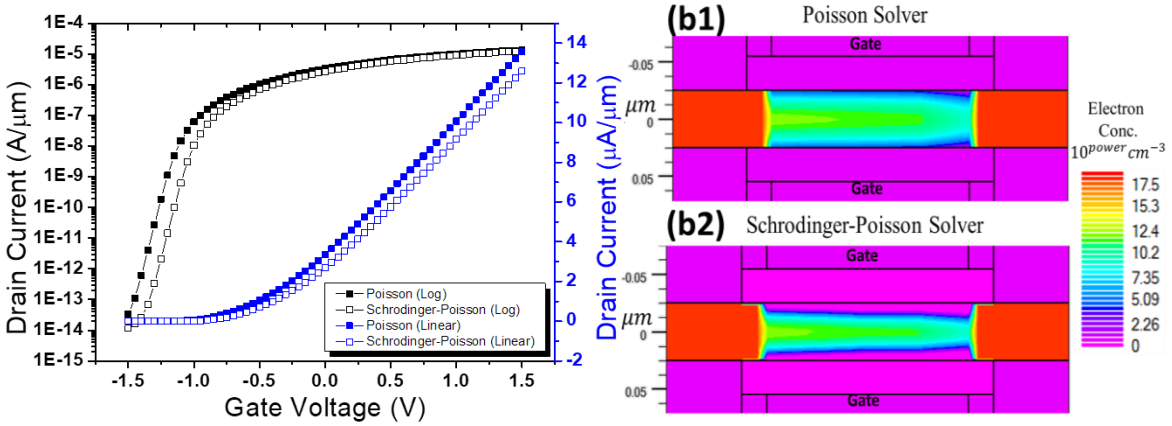
(a) (b)

Fig. 6-3: Effect of Single Gate Vs Double Gate on the (a) transfer characteristics and the corresponding (b) Channel electron concentrations contours at V_{GS}=-1.5V for (b1) single gate (b2) double gate.

6.2.3. Influence of Quantum Effects on Current Density

The influence of the quantum effects on the current density of the simulation was studied by solving the structure with both the Poisson and Schrodinger-Poisson equation. The transfer characteristics of the JLFET from solution of Poisson equation and Schrodinger-

Poisson equation is shown in Fig. 6-4(a). The electron concentration for the two cases at V_{GS}=-1.5V is shown in Fig. 6-4. As shown in Fig. 6-4(b1), the Poisson equation overestimates the carrier density closer to the oxide-semiconductor interface compared to Schrodinger-Poisson equation Fig. 6-4(b2), consequently resulting in a maximum difference of ~7.2% in the I_{DS} of the JLFET. Therefore, Schrodinger-Poisson solver was used for further simulation.



(a) (b)

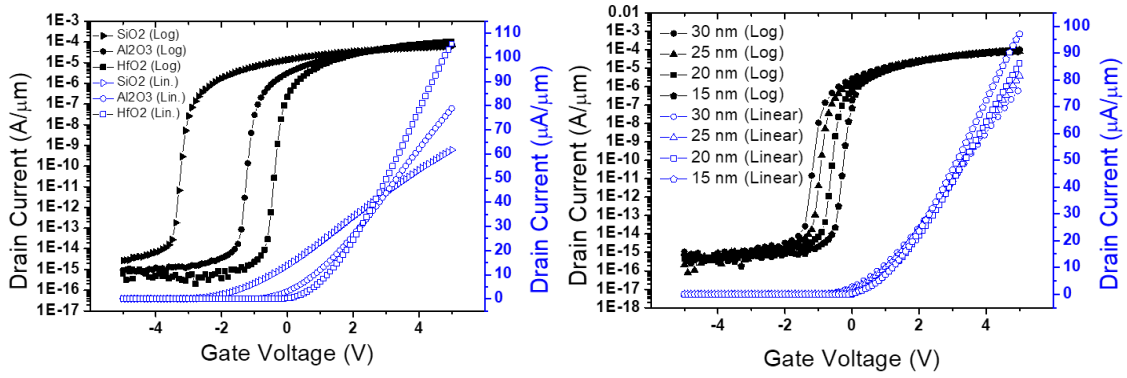
Fig. 6-4: Effect of quantum effects on the (a) transfer characteristics and the corresponding (b) Channel electron concentrations from solution to (b1) Poisson equation and (b2) Schrodinger-Poisson equation at V_{GS}=-1.5V.

6.2.4. Effect of Dielectric Material

Higher the dielectric constant of the gate dielectric more will be the effective control of the gate on the channel. This is well evident from the transfer characteristics shown in Fig. 6-5(a). The gate control increases in the order of silicon dioxide (SiO_2), aluminum oxide (Al_2O_3) and hafnium dioxide (HfO_2), with relative dielectric constants 17.8, 9.3, 4.9 respectively. Interface oxide charge densities of $5x10^{12}$,$-1x10^{11}$ and $1x10^{10}$ which are typical values for the above dielectric materials respectively[261,262]. The best performance was obtained with HfO_2 as a gate dielectric. Since, the practical fabrication was carried out using ALD deposited Al_2O_3 for further simulation Al_2O_3 is considered as a gate dielectric material.

6.2.5. Effect of Dielectric Thickness

ALD deposited Al_2O_3 dielectric has a typical breakdown field strength of 4.4 MV/cm[263]. This implies that a 15 nm gate dielectric, corresponding to an effective oxide thickness (EOT) of 6.29 nm, can withstand to 6.6 V. To achieve higher current, the next set of simulations have been done in the gate voltage range (V_{GS}) of -5 V to +5 V with the drain voltage (V_{DS}) at 5V. For further discussions, I_{D+} and I_{D-} is considered as the drain current at V_{GS} of -5 V and +5V, respectively. Normally-off transistors are the preferred transistors for CMOS circuits and most other applications. The transistor should be off at 0 V. The ON current (I_{ON}) here corresponds to the current at V_{GS}=5 V which is same as I_{D+}. For normally-off transistor, i.e. enhancement mode MOSFET, the OFF current (I_{OFF}) corresponds to the current at 0 V. On-to-off ratio is a critical performance figure of merit for major applications.



a b

Fig. 6-5: Effect of dielectric (a) material and (b) thicknesses of Al_2O_3 dielectric on the transfer characteristics at V_{DS}=1.5V.

Fig. 6-5(b) shows the effect of the Al_2O_3 gate oxide thickness on the transfer characteristics. Decreasing the gate oxide thickness results in increase in gate capacitance which causes higher drive current as well as the higher on-to-off ratio. However, lower dielectric thickness will result in higher tunnelling current which is not considered in this simulation but must be considered for practical fabrication.

6.2.6. Effect of Workfunction

Fig. 6-6 shows the effect of the work function of various gate metals on the transfer characteristics. Change in work function causes shift in the transfer characteristics. This shift leads to significant changes in the on-to-off ratio. Fig. 6-6 inset shows the on-to-off ratio for three different metals namely Ti, Ni and Pt corresponding to the work function of 4.3 eV, 5.15 eV and 5.7 eV, respectively with respective on-to-off ratio of 20.2, 260 and $4x10^7$. Using Pt as a gate material a normally off, depletion mode nanoribbon-based n-type JLFET could be realised.

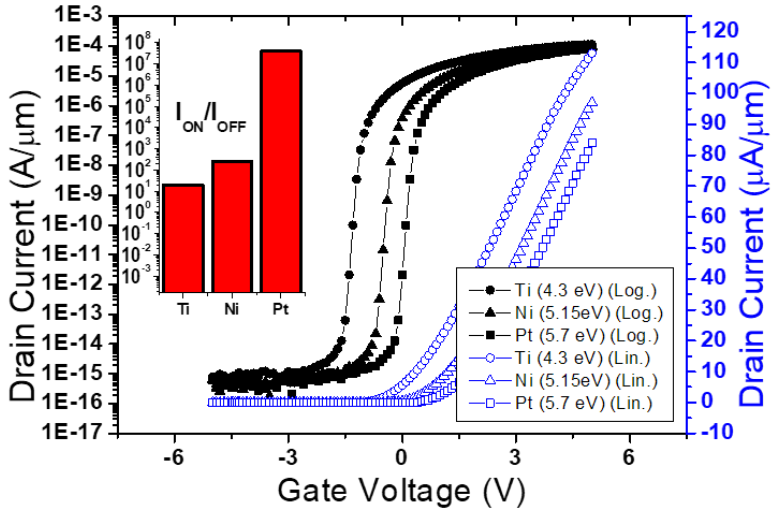
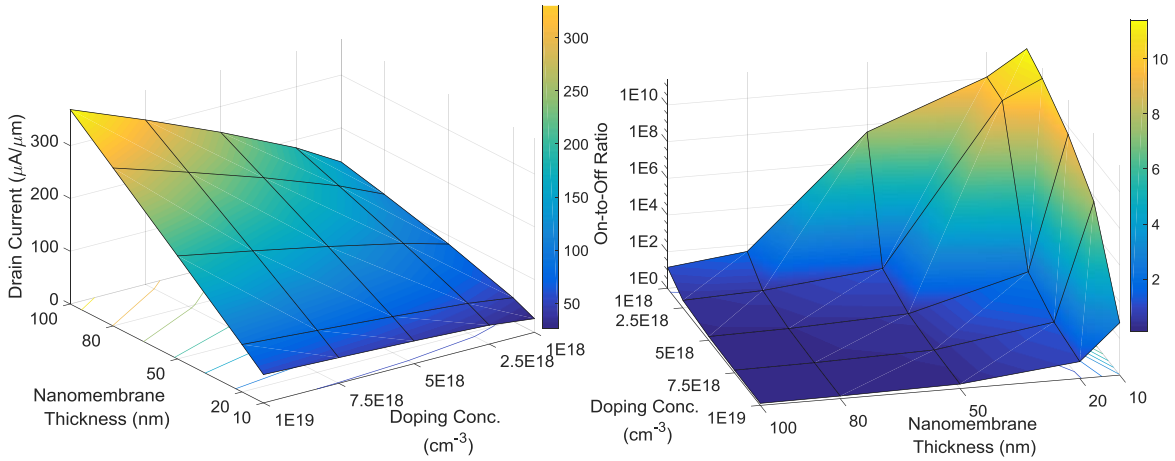


Fig. 6-6: Effect of work function on transfer characteristics (Inset: On-to-off ratio for three different work function).

6.2.7. Effect of thickness of the Nanoribbon and Doping

The thickness of the nanoribbon was varied between 10 to 100 nm and the doping concentration was varied between 10^{18} to 10^{19} cm^{-3}. Fig. 6-7(a) shows the effect of the thickness of the nanoribbon and the doping on the I_{ON} current. Thicker the nanoribbon and

higher the doping more the I_{ON} current. However, as shown in Fig. 6-7 (b), the on-to-off ratio decreases with thicker nanoribbon and higher doping. This is because of increase in the off-state leakage current as the gate is not able to completely deplete the channel. For optimal performance, thinner the nanoribbon thickness is higher the possible value for doping concentration to achieve higher on current with sufficient on-to-off ratio. For nanoribbons of thicknesses 10, 20 and 50 nm, the doping should be less or equal to $7.5x10^{18}$, $4x10^{18}$ and $2x10^{18}$, respectively to achieve higher current with on-to-off ratio $>10^6$. However, the doping cannot be lowered further than 10^{18} cm^{-3} as it should be in the degenerate regime to get ohmic contact in the source and drain region. With a nanoribbon thickness of 50 nm, a doping concentration of 10^{18} cm^{-3}, an Al_2O_3 thickness of 15 nm and Pt as gate material results in a current of 84 µA/µm. This leads to a current of 3.36 mA for a 40 µm channel width.



(a) (b)

Fig. 6-7: Effect of thickness of the Nanoribbon and Doping on the (a) ON current and (b) On-to-off ratio.

6. 3. Fabrication and Characterisation of NR-JLFET

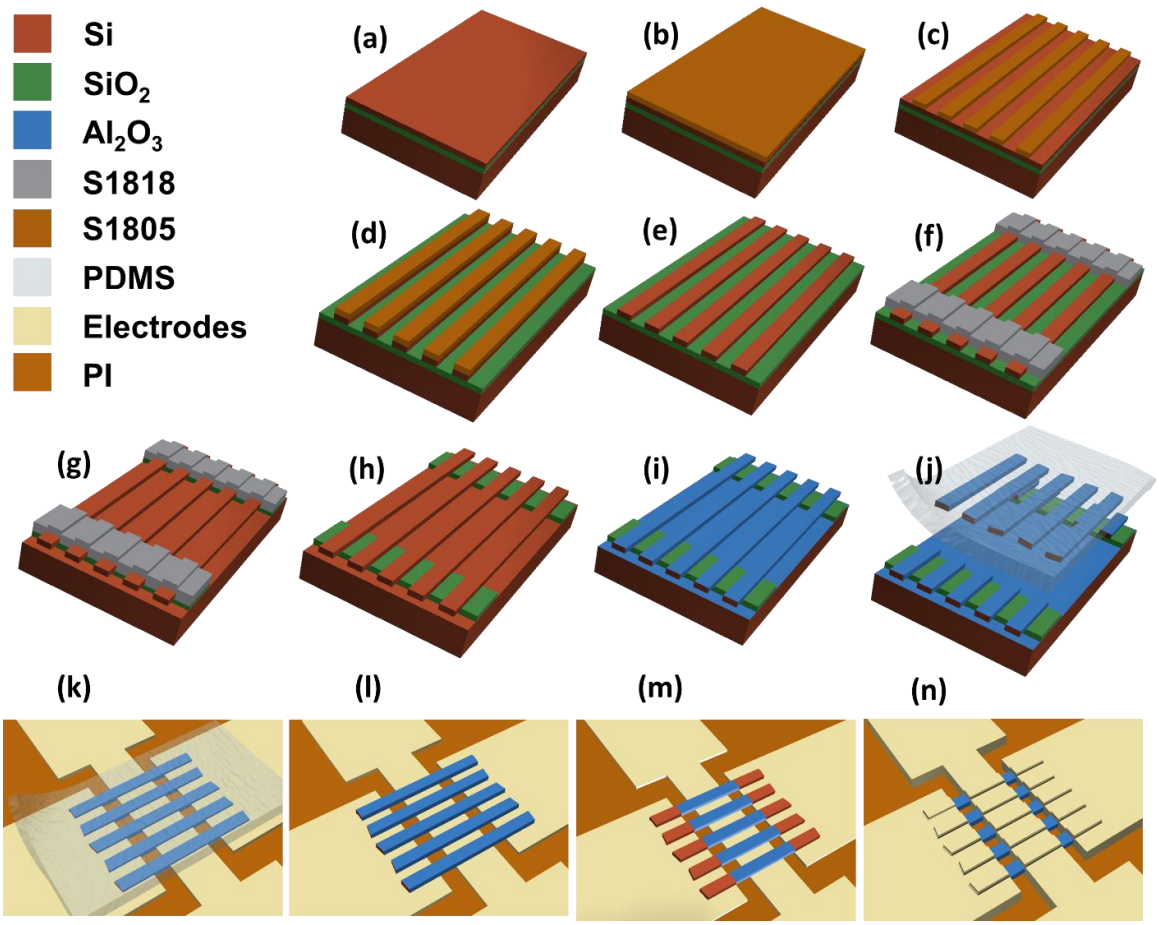


Fig. 6-8: Fabrication steps of Si NR-JLFET

Fig. 6-8 illustrates the steps involved in fabrication of NR-JLFET. While the nanoribbons could be fabricated from bulk silicon wafer, here as a proof-of-concept implementation, SOI wafer has been used to realize the nanoribbons. Fig. 6-9(a) shows the optical microscopic image of various stages of the fabricating and transfer printing process of nanoribbons. The key challenge is to achieve the gate dielectric material deposited all around the nanoribbons and realising the wrapping of the gate around the nanoribbons. The processes were carefully designed so as to achieve the above two goals. SOI wafer with top silicon thickness of 70 nm, oxide thickness of 2 µm and substrate thickness of 600 µm was used to realize silicon nanoribbons (Fig. 6-8a). The ribbons used for study were patterned to have 5 µm width with 5 µm spacing between them (Fig. 6-9 (a1)) with S1818 as the photoresist as per the photolithography recipe described in section 3.1.1.1. The wafer was cleaned with Piranha solution (H_2SO_4:H_2O_2 4:1) for 3 minutes followed by HF solution (100:1) for 1 minute to remove the oxide formed. The wafer was loaded in a thermal diffusion furnace and was doped as desired (Details given in next section). Then photolithography was carried out to define patterns in S1805 positive photoresist (~0.5 µm thick) of 5 µm width with MA/BA6 mask aligner from Suss MicroTec as shown in Fig. 6-8c. The sample was baked in 120˚C for 40 minutes in a convection oven followed by O_2 plasma treatment at 120 W RF power for 2 minutes. Then the ribbons were realised by etching the exposed area in a solution of nitric acid, ammonium fluoride and water in a ratio of 126 HNO_3 : 60 H_2O : 5 NH_4F [264] for 1 minutes 30 seconds. The solution etches the silicon which is not protected by the resist. The etching solution has the etch rate of ~150 nm/minute. The sample was processed for 90 seconds in this solution. The sample was purposefully over etched to make sure that silicon

completely etched which is important to achieve the following step successfully. This was followed by removal of photoresist in acetone kept in ultrasonic bath followed by cleaning in isopropanol (IPA) and de-ionised (DI) water. The next step is to remove the oxide from beneath the ribbon structures so that the ribbon will be hanging between lithographically defined anchor points. To achieve this, the wafer was coated with a S1818 photoresist followed by a second lithographic patterning (Fig. 6-8f) to realize anchoring structures of the ribbons. The sample was then hard baked at 120^{o}C for 35 minutes in an oven followed by O_2 plasma treatment at 120 Wt RF power for 2 minutes. The wafer was etched in 5:1 buffered oxide etchant for 35 minutes. The etchant removes the oxide in between and underneath the ribbons to make them hang between the anchor points defined by the second lithography (Fig. 6-8(g)). This etching is critical to completely release the ribbons from the oxide underneath. Then the wafer with the hanging ribbons are immersed in acetone (without ultrasonic bath) to remove the photoresist followed by IPA rinse and DI water rinse. Fig. 6-9(a2) shows the released ribbons hanging between the anchors.

Atomic Layer Deposition (ALD) was used to deposit Al_2O_3 high-k dielectric layer of 30 nm over the hanging ribbons. The ALD deposition was carried out at 200˚C for 300 cycles. The gap between the anchors is critical as having a larger gap will make the hanging ribbons to touch the bottom substrate eventually forming a bond during the ALD process. Once the bond forms, the ribbons cannot be released in these areas from the substrate and gets broken in between. The results corresponding to the optimisation of this gap between anchors are shown in Fig. 6-9(b). Fig. 6-9(b1) shows SEM image of the ribbons hanging between anchor structures with increasing gaps between anchors from left to right. The ribbons (>= 65 µm gap) on the right are touching the base Si as observable from the SEM image. The fabricated ribbons were transfer printed to PI foil using an intermediate PDMS stamp (Prepared from Sylgard 184 (10:1) at 80^{o}C) similar to that used for UTC transfer (depicted in Fig. 6-8 (j)). Before stamp printing, the PDMS stamp and the ribbon sample was treated in oxygen plasma at 150 W for 20 seconds and then brought in contact with each other. A gentle pressure of ~50 kPa was applied on it to make the PDMS stamp form a conformal contact with the ribbon sample. Then the PDMS stamp was gently removed to detach the ribbons from the source SOI wafer. The ribbons break in the anchor point. Fig. 6-9(a3) shows the anchors after the ribbons are removed by the PDMS stamp. Fig. 6-9(a4) shows the images of the ribbons transferred to the intermediate PDMS stamp. A final transfer of ribbons are carried out to the target PI substrate.

The PI substrate was prepared as follows. PI 2545 from HDmicrosystems was spun on a glass wafer. The adhesion between glass wafer and PI was promoted by coating VM652 at the periphery in a discontinuous fashion. The discontinuous gaps in the layer facilitates the flow of gases formed during PI curing process. The pre-cure PI solution is spun on the glass wafer at 5000 rpm for 120 seconds. At 5000rpm the thickness of PI is 1.5 microns (PI 2545 datasheet). To achieve the thickness of ~10 microns, the PI was spun 7 times with the same speed. Then, PI film was cured at 150^{o}C for 60 mins on a hotplate and then hard-cured at 250^{o}C in the N_2 oven. Fig. 6-9(a5) shows the ribbons finally transferred to the polyimide substrate from the PDMS stamp. As seen in Fig. 6-9(b2), only ribbons <65 µm are successfully transferred while ribbons above this dimension breaks in the middle or is not transferred at all. This is further evident from the transferred ribbons shown in Fig. 6-9(c1 to c3).

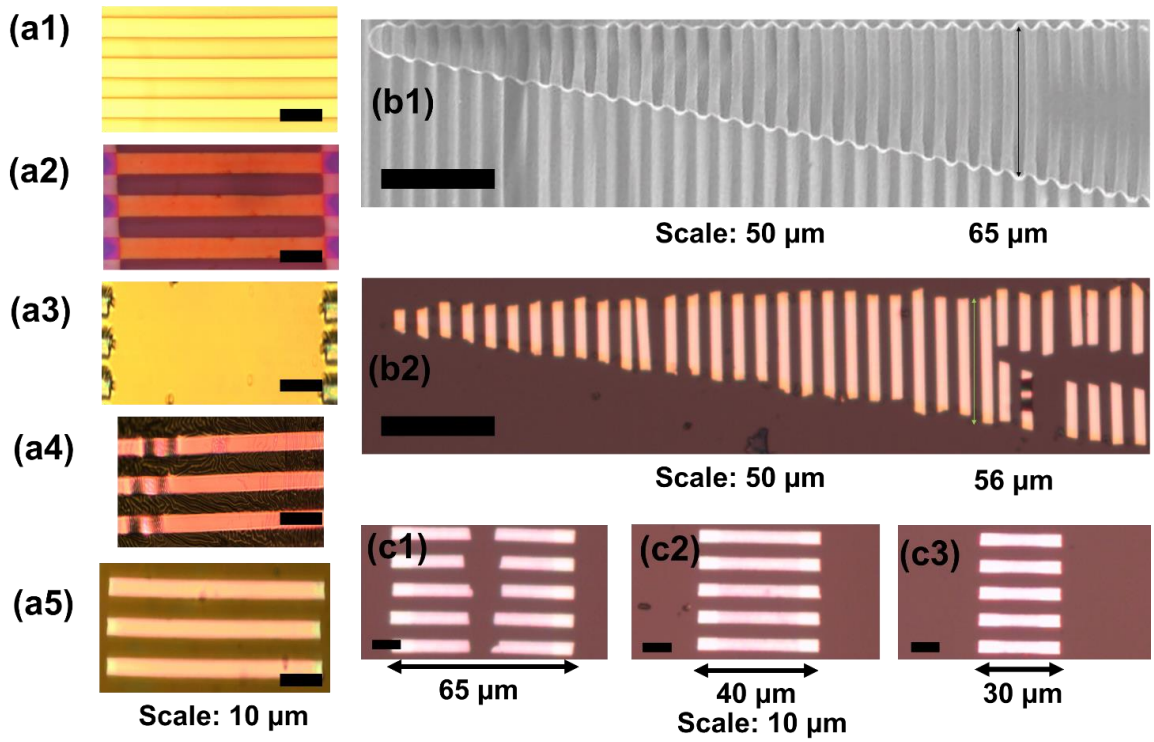


Fig. 6-9: (a) Optical microscopic image of various stages of the synthesis and transfer printing process of ribbons (a1) Pattern definition of ribbons (a2) Released ribbons hanging between the anchors (a3) Anchors after the ribbons are removed by PDMS stamp (a4) Ribbons transferred to the intermediate PDMS stamp (a5) Ribbons finally transferred to the polyimide substrate from the PDMS stamp. (b) Optimisation of gap between the anchor points (b1) Scanning Electron Microscopic image of hanging ribbons between anchors of various dimension. (b2) Optical microscopic images of ribbons transferred to receiving polyimide substrate via a intermediate PDMS stamp. (c) Arrays of transferred ribbons of length (c1) 65 µm (c2) 40 µm and (c3) 30 µm

For device fabrication, the electrodes were defined by lift-off on the top of the polyimide before stamp printing the electrodes were defined by lift off (Fig. 6-8(k)). After ALD, stamp printing process was used to transfer the ribbons from the SOI substrate to the metal patterned target polyimide film (Fig. 6-8 (j) and Fig. 6-8 (k)). Then the ribbons were transferred to the receiving substrate with patterned electrodes (Fig. 6-8(k)). VM652 adhesion promoter was used to increase the adhesion between the PI substrate and the nanoribbons. Then the dielectric on the source and drain regions were removed (Fig. 6-8 (m)). This is followed by definition of source, drain and gate electrodes with liftoff process which complete the fabrication of the JLFET. The JLFET on PI were annealed at 350˚C for 30 minutes in a forming gas ambient (N_2+4% H_2). The source/drain and gate electrodes can also be defined separately if different metals are required for source and drain. For the initial fabrication, titanium was used as a metal for all three electrodes.

6. 4. Nano-ribbon JLFET Results and Discussion

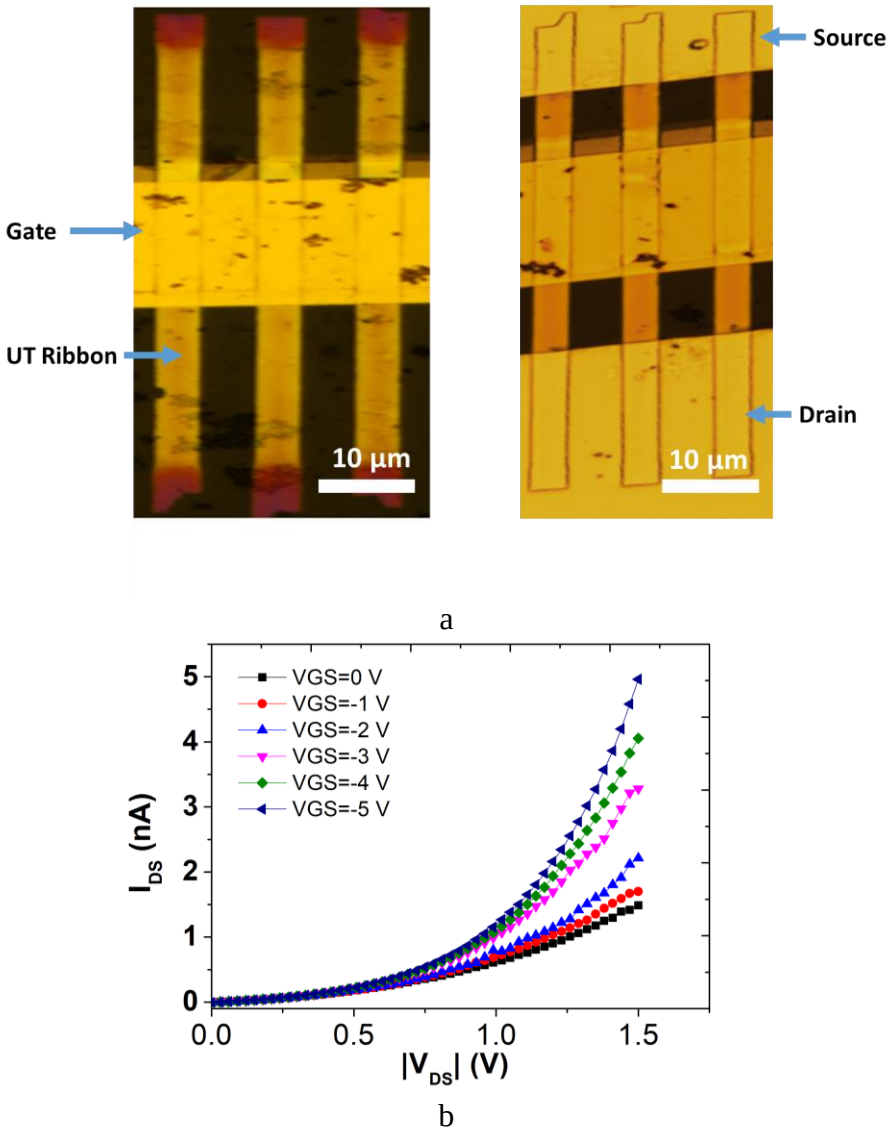


Fig. 6-10: (a) Optical microscopic images of SiNR-based JLFET before and after source drain metallisation for different processes. (b) V_{DS}-I_{DS} characteristics before sintering.

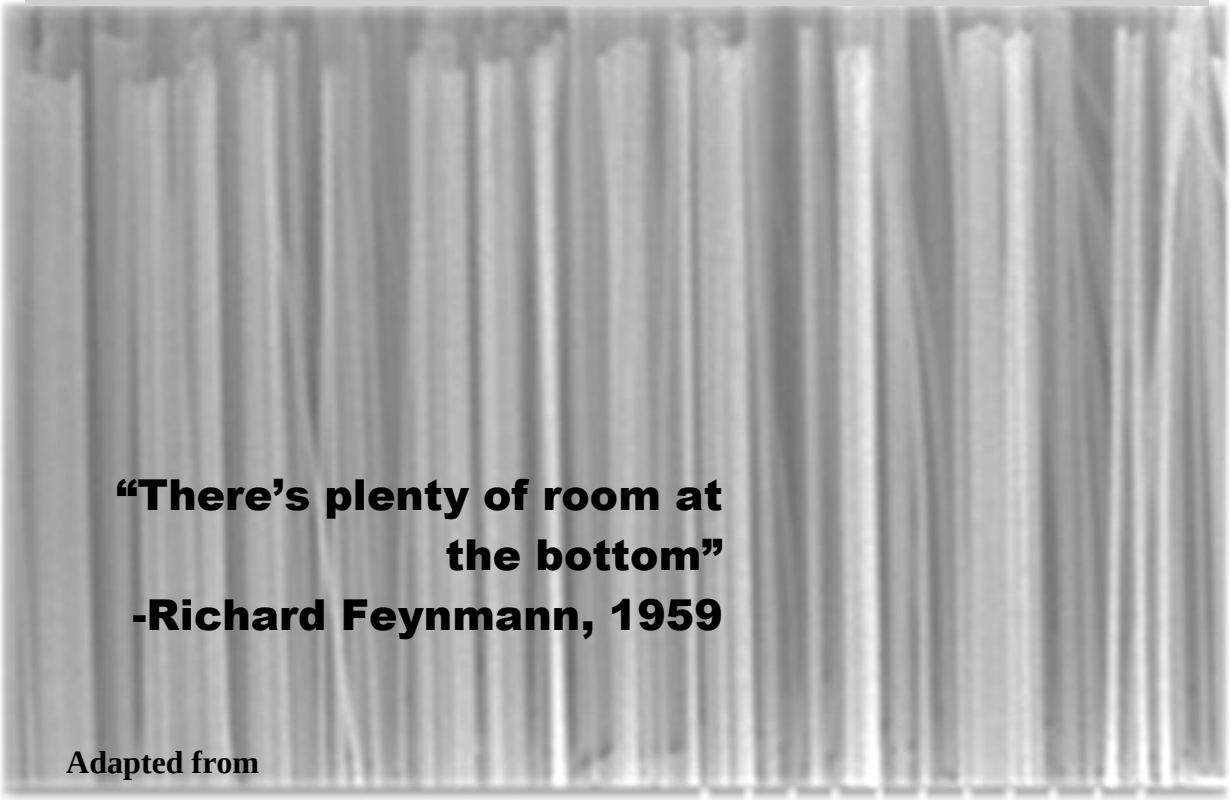
Fig. 6-10(a) shows the fabricated SiNR-based JLFET before and after source drain metallisation. The device fabrication is a work-in-progress. Aligned transfer printing of ribbons to electrode is yet to be optimised as observable in the angular misalignment. Fig. 6-10(b) shows the drain-source voltage vs drain current characteristics for various gate voltages before the device sintering. While there is a clear field-effect observed (change in I_{DS} with V_{GS}), the drain current observed is far low (in nA) compared to the expectation from simulation (in mA) range. The potential reason could be that the etching of the gate dielectric in the source and drain is not sufficient which has resulted in a poor source-drain contact. Forming gas annealing (FGA in 5%H_2 in N_2) at 350ºC for 30 minutes was carried out to improve the contact however the PI film disintegrated during this process resulting in all the electrodes getting damaged. All the above disparities are currently being optimised in ongoing process iterations.

6. 5. Summary

In summary, TCAD simulation study of SiNR-based JLFET devices presented in this chapter shows that they have the high-performance and hold promise for solving the doping related challenges in flexible and printable electronics. The device structure presented here can drive micro LEDs which typically require high drive current. Based on the simulation based optimisation, a current of 3.36 mA for a 40 μm channel width is achievable with an on-to-off ratio of 4.02x 10^7. The use of metal gate provides a promising alternative for flexible electronics application compared to polysilicon gate conventionally used for JLFET[258]. The transfer printing of nanoribbons has been optimised for fabrication of JLFET. The low current observed in the fabricated JLFETs indicate that the contact has to be optimised for better performance. Nevertheless, the observed field-effect (gate voltage's influence on the drain current) and the simulation-based optimisation indicates that flexible JLFET could be considered as one of the promising candidate for high-perfomance flexible electronics. Further investigation in this direction is currently in progress.

7

Nanowires



“There’s plenty of room at the bottom”
-Richard Feynmann, 1959

Adapted from

W Navaraj, D Shakthivel, C Garcia Nunez, F Liu, D Gregory, R Dahiya, Metal-Assisted Chemical Etched Si Nanowires for High-Performance Large Area Flexible Electronics, InnoLAE 2017, Cambridge, UK.

C. G. Nuńez[#], W. T. Navaraj[#], F. Liu, D. Shakthivel, R. Dahiya, "Large-Area Self-Assembly of Silica Microspheres/Nanospheres by Temperature-Assisted Dip-Coating", ACS Appl. Mater. Interfaces 2018, 10, 3058−3068, [#]Equal Contribution, Copyright 2018 American Chemical Society.

CG Núñez, F Liu, WT Navaraj, A Christou, D Shakthivel, R Dahiya, Heterogeneous integration of contact-printed semiconductor nanowires for high-performance devices on large areas, Nature: Microsystems & Nanoengineering 4 (1), 22, 2018, CC BY 2.0.

Contents

7. Nanowires

An illustration of various stages in fabricating high-performance flexible electronics by printing of nanowires is shown in Fig. 7-1 which typically involve synthesis, transfer printing [20,265] and fabrication of electronics. The following are the reasons why nanowires are considered as potential candidate for large-area electronics from nanowires:

- Higher Mobility
  - Non-porous <100> crystalline nanowire with higher material compared to organic materials
- Flexibility
  - Inherent
- Large Area processable patterning/registration
  - Printing Sub-30 nm heavily doped nanowires
- Lower Cost
  - MACE Process
- Circuit Architecture
  - Array architecture

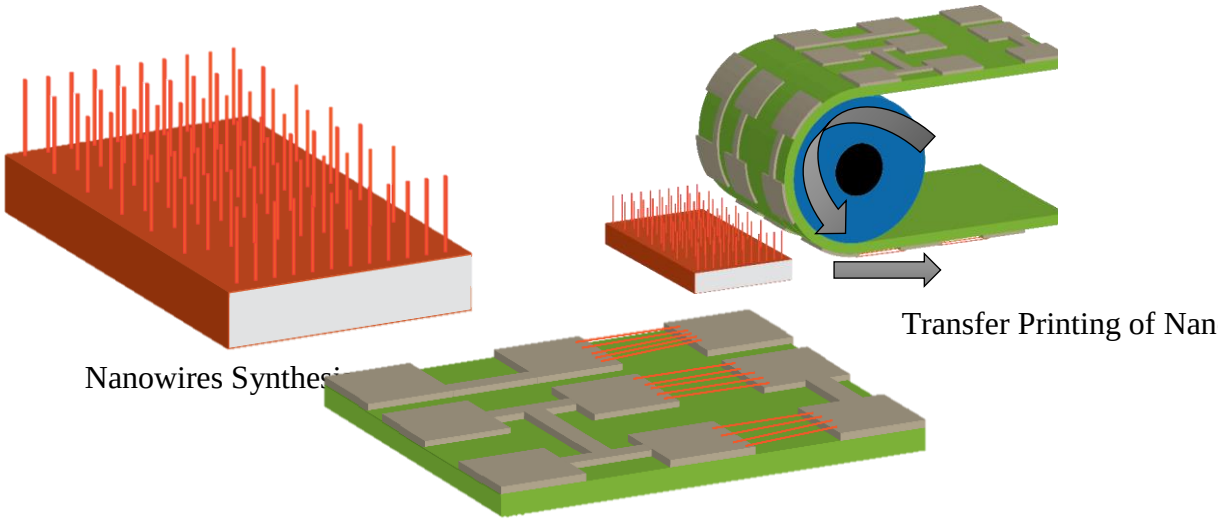
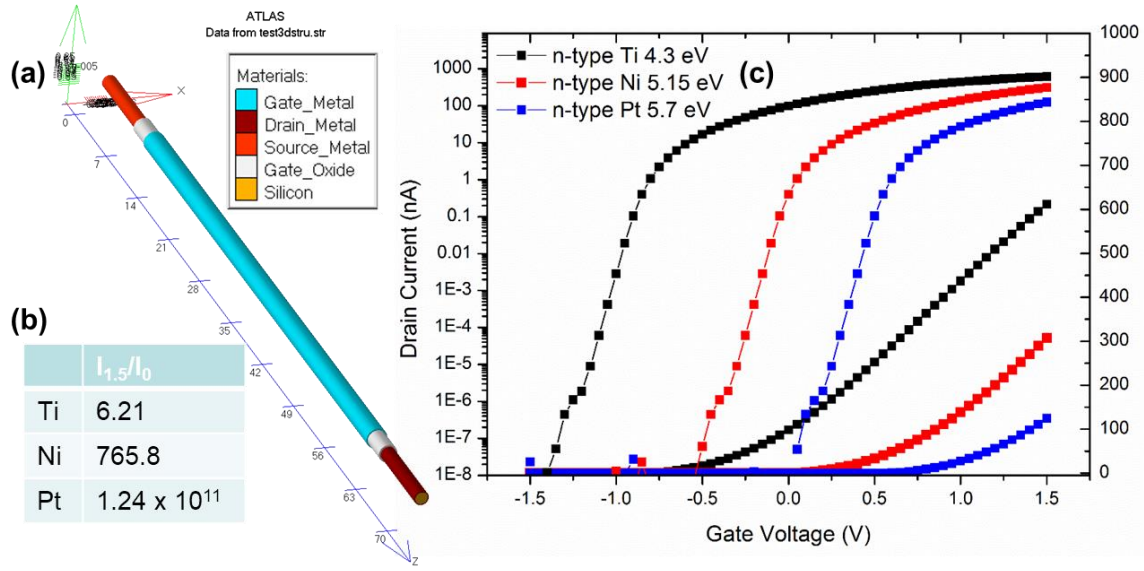


Fig. 7-1: Illustration of various stages in fabricating high-performance flexible electronics by printing of nanowires

7. 1. Simulation of JLFET based on NWs

Similar to nanoribbons as presented in previous chapter, JLFET strategy could be useful for realising FETs from nanowires specially to avoid the need for controlled source-drain doping. To achieve this, it is required to realize sub-30 nm nanowires for complete control of channel region and using work function of the metal to turn off the channel as presented in section 6. 2. and observed from the simulation result below. The rest of the parameters and models were considered similar to that of nanoribbon based junctionless FET simulation. The nanowire was of diameter 30 nm with Al_2O_3 dielectric of 10 nm thickness surrounding the nanowire and gate electrode of 50 nm thickness surrounding 270˚ across the nanowire. The source and drain electrodes spanned 10 µm in length while the channel was of 50 µm length. The carrier concentration of the channel was considered as 10^{19} cm^{-3}.



	$I_{1.5}/I_0$
Ti	6.21
Ni	765.8
Pt	1.24 x 10^{11}

Fig. 7-2: (a) Simulated structure (not to scale). The gate was covered only upto 270 degree to resemble processing coverage (b) Drain current ratio ($I_{@VDS=1.5}$:$I_{@VDS=0}$) (c) Transfer characteristics for three different gate metals.

As observed for nanoribbon FET, normally-off JLFETs with nanowire are achievable by gate work function control with on-to-off ratio of more than 10^{11} achievable with this approach. The following section describes strategies for synthesising nanowires.

7. 2. Synthesis of Nanowires

Metal-assisted Chemical Etching (MACE) is emerging as a powerful nanofabrication technique [266]. Feature resolutions on the order of nm to µm with depths in the order of tens of microns has been achieved using MACE resulting in very high aspect ratio. MACE has been used for etching micron and nano-sized structures into Group IV, Group III-V, and Group II-VI semiconductors [267,268]. The optimal parameters for MACE are discussed initially in this section:

7.2.1. Optimal MACE etching parameters

MACE process depends on several processing as well as structure-related parameters such as chemicals/concentration, catalytic metal, doping, temperature, mesh dimensions etc as illustrated in Fig. 7-3. The desired outcome is non-porous, crystalline, smooth nanowires of desired length, diameter and doping. As a part of it, a code has been developed in matlab based on empirical results from literature [147,266] and some experiments. The aim is to predict the general trend to find the depth of etching, orientation and whether the film will be porous or not for a given time, concentration and temperature. Further attempts are being made to incorporate the time varying rate observed during MACE for higher concentrations.

Fig. 7-4a sums up the result as surf plot indicating etch rate at various molar concentrations for MACE on n-type Si (100) wafers with resistivity of 10 Ω·cm with a 20 nm thermally evaporated gold film deposited at a rate of 2.1Å/s. Fig. 7-4b gives the MACE etch rate for similar molar concentration range as in for sputtered Au/Ag bilayer film with 15nm thick Ag followed by 5nm thick Au film pattern achieved through an Anodic Alumina Oxide (AAO) template[147]. The etch rate is high when both HF and H_2O_2 concentration is significant. The reason for this could be understood considering the mechanism of catalytic MACE etching illustrated in Fig. 7-6. The catalytic metal and the surrounding

silicon forms a local electrochemical cell. The reactions happening within the local electrochemical cell is also shown in Fig. 7-6. The net effect is that H_2O_2 oxidises the Si while HF etches the silicon. The reaction is much pronounced underneath the metal catalyst which results in release of H_2 and hexafluorosilicic acid (H_2SiF_6). This results in chemical free energy converted into mechanical propulsive energy which pushes the catalytic metal further underneath. The process continues as the MACE progresses. Fig. 7-4c shows the various region within the concentration distribution where the MACE process may result in porous structure (red region), <110> oriented nanowires (blue region) or peel-off of the etching film (green region) and intermediate regions. At low HF concentration (green region) the H_2O_2 oxidation dominates where the nanomesh is observed to peel-off. In the region where the HF and H_2O_2 concentration are comparable, it is resulting in porous nanowires. For region near 10M H_2O_2 and 15M HF (blue region), <110> nanowires are obtained. Black corresponds to region where we get non-porous and <100> oriented nanowires.

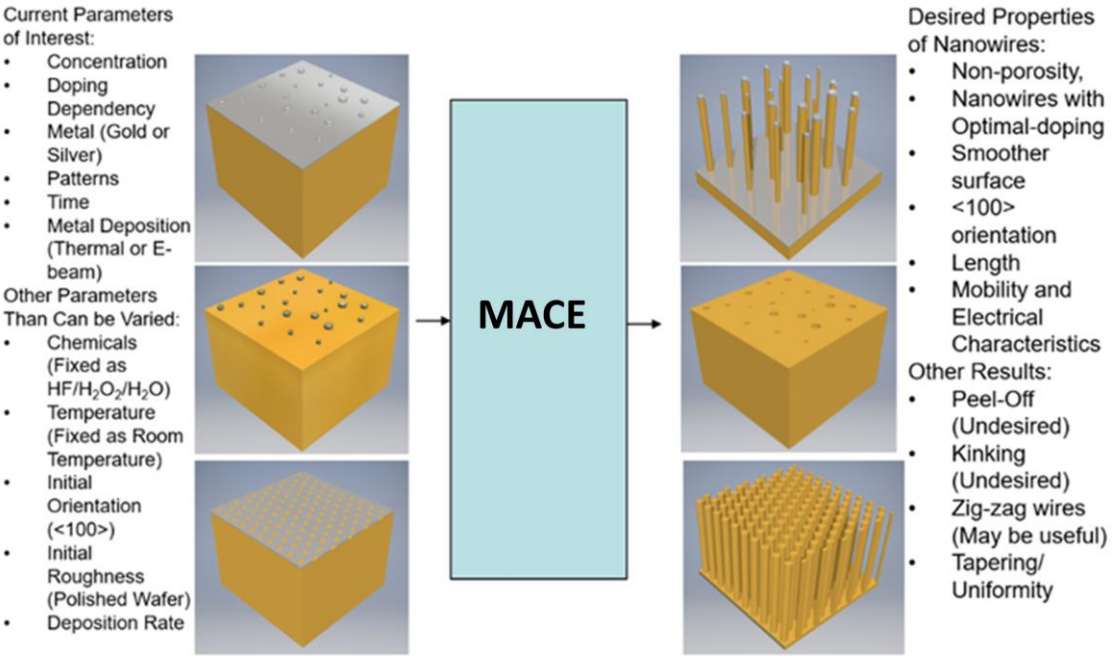
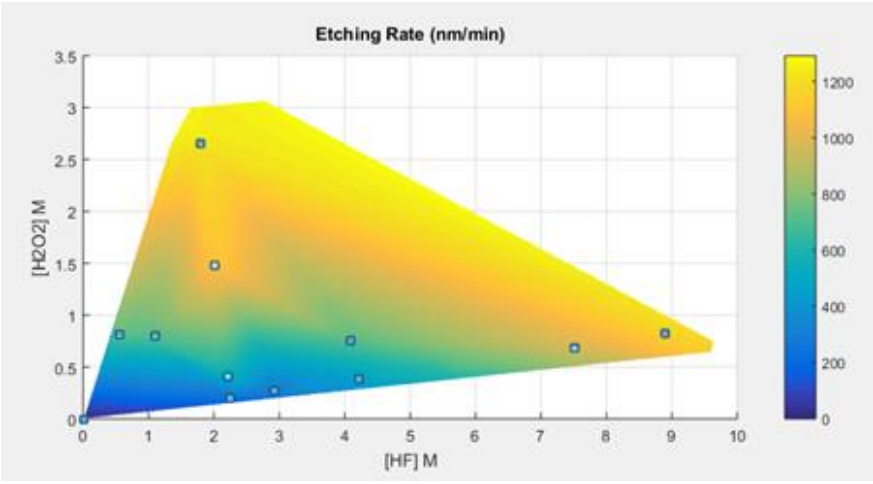


Fig. 7-3: Dependency of MACE on various process related parameters

Normally for MACE, etch rate as a function of concentration of solutions is generally reported in literature based on which the contours are plotted. However, at very high concentration for just Au as catalytic metal, a time varying etch rate was observed. For eg., the results for etching with 14M HF, 3M H_2O_2 is shown in Fig. 7-5. The figures (a-d) corresponds to the cross-sectional SEM image of evolution of MACE for a 14M HF, 3M H_2O_2 concentration for 0 Mins, 2 Mins, 15 mins and 20 mins respectively. The rear side of the wafer is indicated by the dashed lines. It is observed that there is no noticeable etch after 2 mins other than a porous layer formation underneath the metal mesh. Fig. 7-5(c, d) shows the top part of the nanowires after 15 mins etching and 20 mins etching respectively. Fig. 7-5e shows the observed rate vs time and etch depth vs time for this process. A time dependent etching rate was observed. The reason for this could be attributed to continuous increase of porosity of the metal film during etching with high concentration due to the expansion of the pores which causes more chemical species to reach etching site and thereby speeding up the etch rate.



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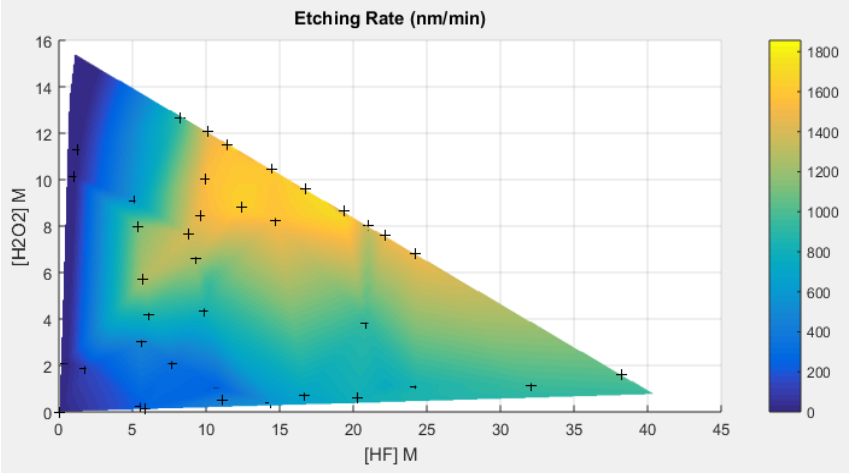

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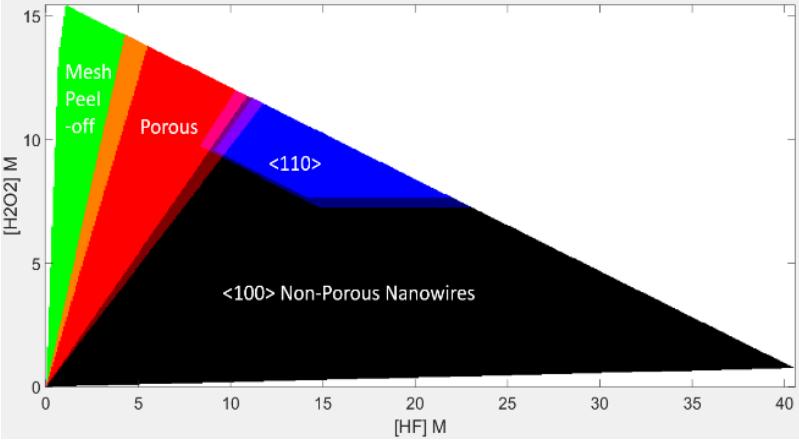


c

Fig. 7-4: Surface plot of etch rate for MACE at 20°C for (a) gold [266] (Blue points indicate the empirical values) (b) For Au/Ag bilayer[147] (Black Crosses indicate empirical values) (c) shows the expanded view for the Au/Ag bilayer system (Black Crosses indicate empirical values) for the complete experiment range (d) shows the various region within the concentration where the MACE process may result in porous structure, <110> oriented nanowires or peel-off of the etching film and intermediate regions.

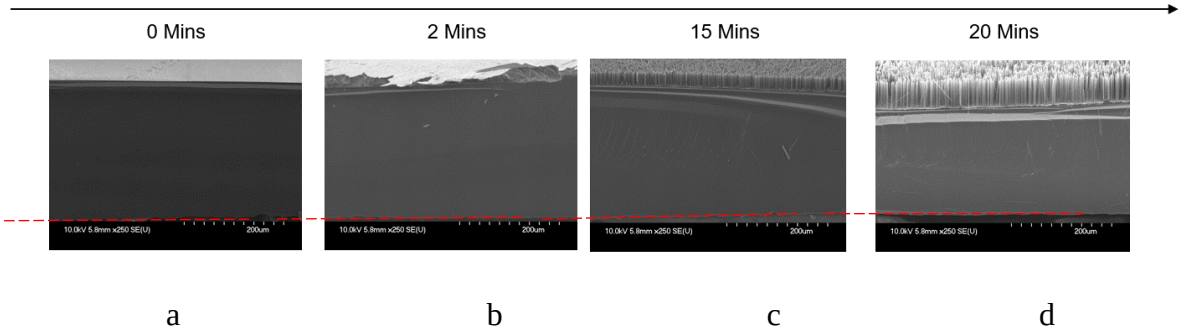


Fig. 7-5: (a-d). Cross sectional SEM image of evolution of Metal Assisted Chemical Etching (MACE) achieved with Nanosphere Liftoff (450 nm diameter porous mesh) seen compared to the thickness of the wafer for d: 0 Mins, e: 2 Mins f: 15 mins and g: 20 mins respectively. The rear side of the wafer is indicated by the dashed lines. The thickness of the wafer is 250 µm.

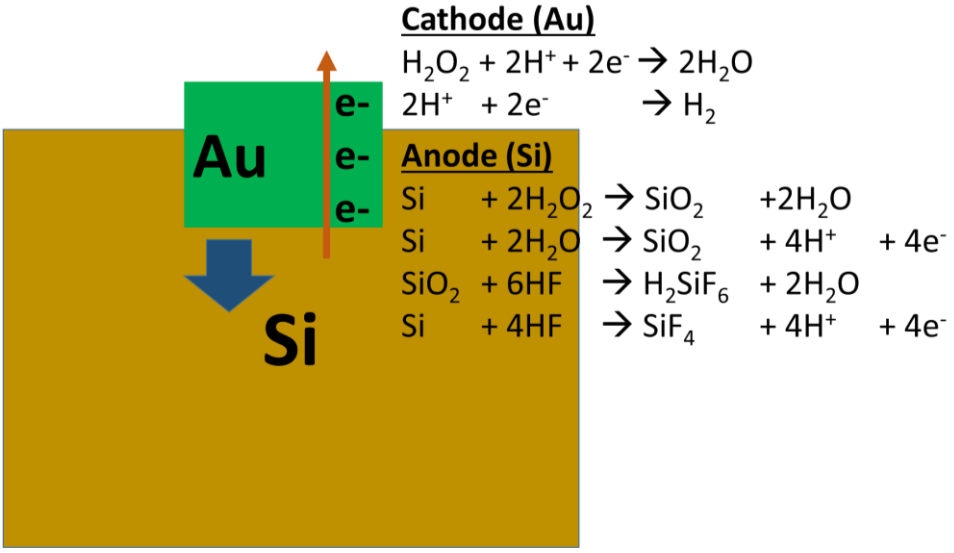


Fig. 7-6: Electrochemical reactions during the MACE process

The typical parameters required for MACE is established above. Four approaches of nanowire synthesis based on MACE has been carried out. The patterning stage varies in each while the MACE process is similar for all cases. This section explains the four approaches.

7.2.2. Metal-Dewetting based Statistically Distributed Patterning followed by MACE

Stage 1: Random/ statistically distributed nano-patterning by metal de-wetting

As illustrated in Fig. 7-7(a) where an ultra-thin layer of metal, is heated above the eutectic temperature, resulting in the continuous film broken into smaller droplets of different diameter depending upon the process conditions. This solidifies on cooling resulting in statistically distributed nano-patterns.

Gold film of ~7nm thickness was deposited in electron beam evaporation system at a rate of 0.3nm/s after pumping the process chamber to a vacuum of ~$1x10^{-7}$ mbar. The film was annealed for 10 minutes at a temperature of 900^{o}C in a nitrogen ambient in a Rapid Thermal Annealing system. This resulted in the formation of metal nanoclusters as shown

in Fig. 7-7e (illustrated in Fig. 7-7(a). A thin film of silver of ~20nm thickness was deposited over the gold nanoclusters in a thermal evaporator system after taking the chamber to a pressure of ~$2x10^{-6}$ mbar.

Stage 2: Metal Assisted Chemical Etching (MACE):

MACE has been carried out in a solution of 4.6 M HF and 2 mM H_2O_2 for ten minutes. This results in metal assisted chemical etching at the silver area compared to gold resulting in nanowires. The process is schematically illustrated in Fig. 7-7b-d. Fig. 7-7f, g and h show the SEM images of the synthesised nanowires. The diameters of the nanowires were in the range from 20 nm to 150 nm with varying heights depending upon the time of etching.

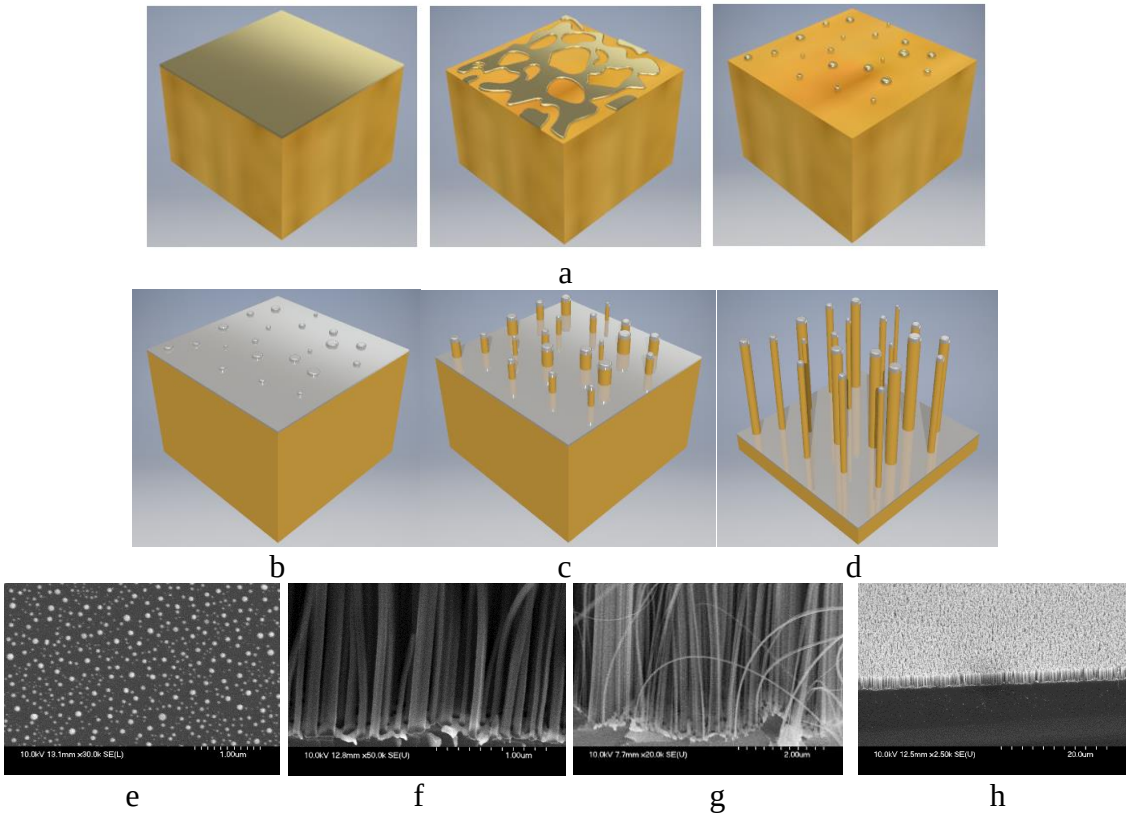


Fig. 7-7: Metal-Dewetting based Statistically Distributed Patterning followed by MACE for nanowire synthesis.a) Dewetting of ultra-thin metal. The metal chosen should have no or lower etching rate in the MACE solution (b) Deposition of a noble metal film (c) and (d) MACE process SEM images of (e) Random nano-clusters formed by metal dewetting (f-h) fabricated silicon nanowires using MACE.

Approach 1 resulted in nanowires of random diameter and ordering. It is a simple and easy method for fabricating nanowires on large area. While metal-dewetting is suitable for large scale facile synthesis of nanowires the significantly more statistical nature of distribution of wires may result in statistical variation in resulting electrical characteristics. In order to get nanowires of controlled density and diameter the initial nano-mesh has to be patterned. The next three approaches present patterning strategies for nanowires synthesis with less statistical variation in terms of diameter and pitch.

7.2.3. Dots-on-the-fly EBL patterning followed by MACE

In the second approach, Electron Beam Lithography (EBL) has been used for synthesising nanowires. EBL is relatively straight forward process which could be used for fabricating nano-mesh patterns with desired diameter, pitch etc. in a controlled way. However, it has disadvantages associated with its cost and it is a slow process. Further, it cannot be used for large area applications. Conventionally, EBL is carried out by designing the desired pattern and then patterning it as explained in section 3.1.1.2. However, instead of designing array of circular patterns, the inherent mechanism in which EBL works can be exploited for speedy writing of nanopatterns known as dots-on-the-fly. This not only increases speed significantly but with this approach the file size required to be handled by the EBL system also goes down significantly. This has been explained in section 3.1.1.2. The process is schematically shown in Fig. 7-8. Here, VB6 has been used to write dots on silicon sample of 50 nm to 100 nm diameter and ~500 nm pitch. Patterns have been designed in L-edit which is followed by use of Beamer to split the file into beaming patterns (a square pattern is shown in Fig. 7-8a). Optimal values for related parameters such as Beam Current, VRU, frequency, field size, dose, and spot diameter were considered to get dots of desired pitch, diameter and good circularity. Fig. 7-9 shows the variation in circularity for different beam current and aperture size shown as A, B and C. The best circularity of 0.91 was obtained for the beam current of 32 nA with 70 μm aperture size as observed in Fig. 7-9(a, b, d). The variations in the size across the field is also lower for the same value. The recipe used for the EBL is tabulated below:

Table 18: Optimised parameters for dots-on-the-fly EBL

Recipe
Tool: VB6 Bottom Layer PMMA: 2010 4% 100nm (Spin: 5k speed, 20k acceleration, 60 s) Top Layer PMMA: 2041 4% 100nm (Spin: 5k speed, 20k acceleration, 60 s) Beam Current: 32 nA Aperture Size: 70 μm Energy: 100 kV Resolution: 1.25 nm VRU: 400 (Resulting 500 nm BSS or pitch) Bake Time: 180˚C 2 hours Developer: (PGMEA:IPA 2.5:1) 30 s @23˚C followed by IPA rinse 30 s

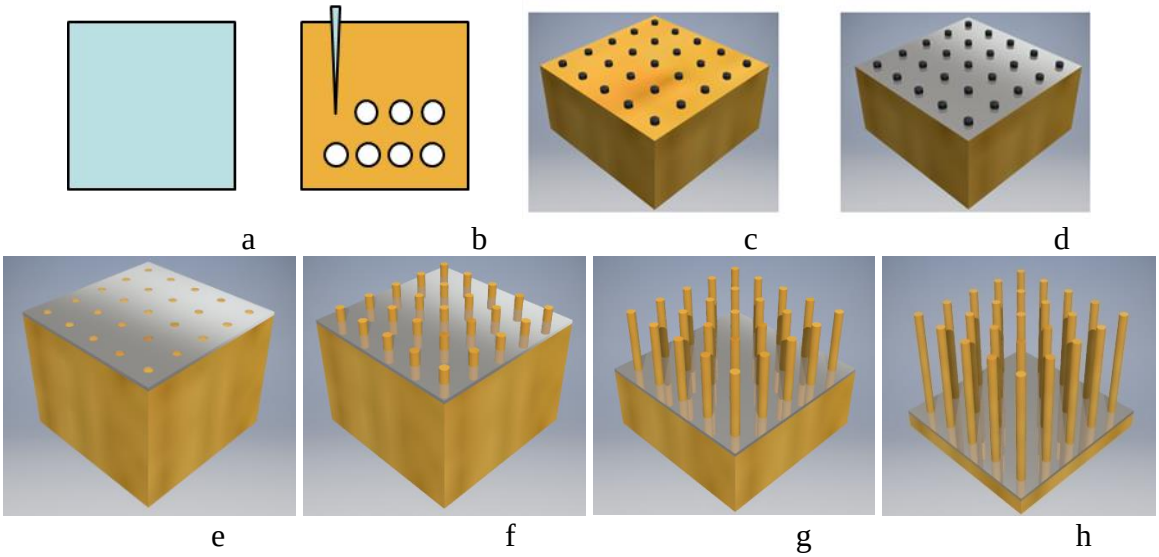


Fig. 7-8: Schematic Illustration of dots-on-the-fly EBL followed by MACE

EBL was done on a PMMA bilayer photoresist spin-coated on a silicon substrate with 100 nm SiO_2 on top. After developing, a 50 nm NiCr was deposited and lift off was carried out to get patterned NiCr dots (Fig. 7-8c). After patterning NiCr dots, with this process a dry etch was carried out to etch the SiO_2 with NiCr as mask. Silver or Gold film of thickness ~20-40nm was deposited with any of the following tools namely, thermal evaporator, e-beam evaporation or the table-top sputtering tool (Fig. 7-8d). The NiCr dots were lifted off by etching the SiO_2 using BOE (5:1) leaving behind a nanomesh(Fig. 7-8e). This is followed by MACE (Fig. 7-8f-h) resulting in the formation of nanowires.

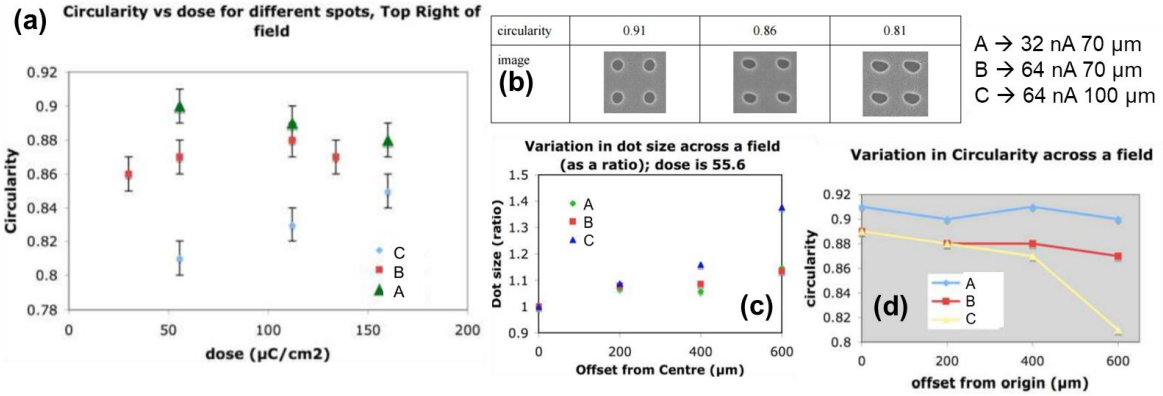


Fig. 7-9: Deciding EBL parameters for optimal circularity of dots

Fig. 7-10 shows the typical dot patterns realised using e-beam lithography where Fig. 7-10(a-b) shows SEM images of E-beam patterns of 100 nm diameter and 500 nm pitch. Fig. 7-10 (c) shows SEM images of patterns of 50 nm diameter and 500 nm pitch. Fig. 7-10(d) shows the AFM scan of dots of the same sample.

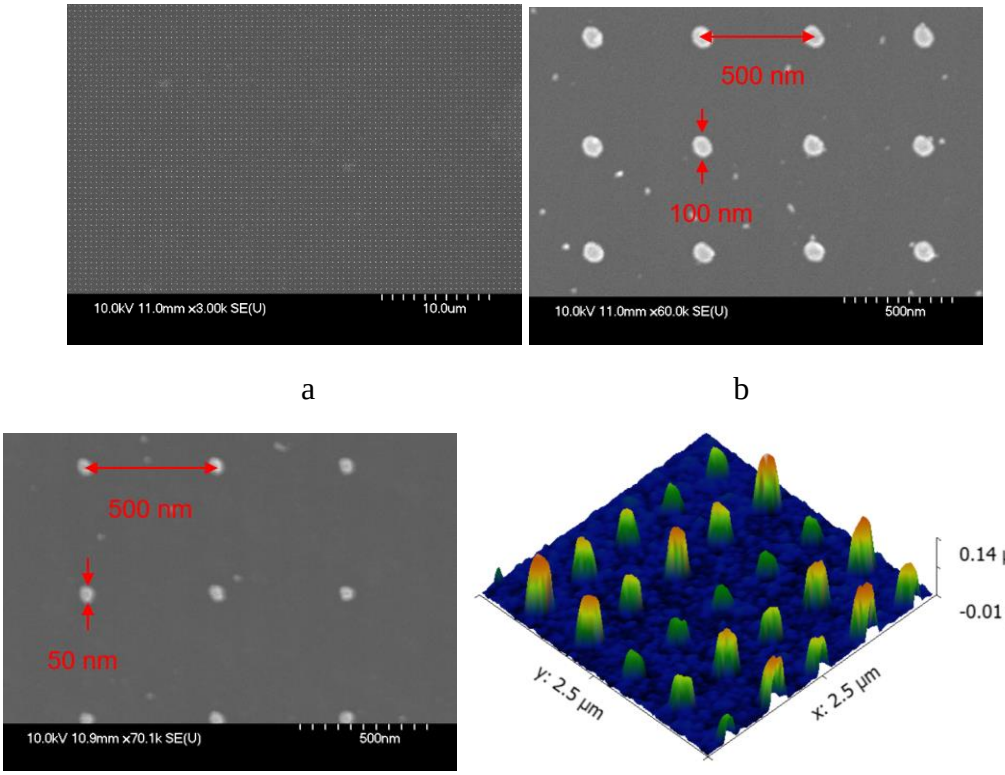


Fig. 7-10: E-beam patterns (a-b) SEM images of E-beam patterns of 100 nm diameter and 500 nm pitch. (c) 50 nm diameter and 500 nm pitch (d) AFM scan of dots of 50 nm diameter and 500 nm pitch.

Fig. 7-11 shows the image of nanowires achieved using MACE from the e-beam lithography patterned samples. The nanowires are of diameter 50 nm and length ~750 nm realised using E-beam patterned nanomesh.

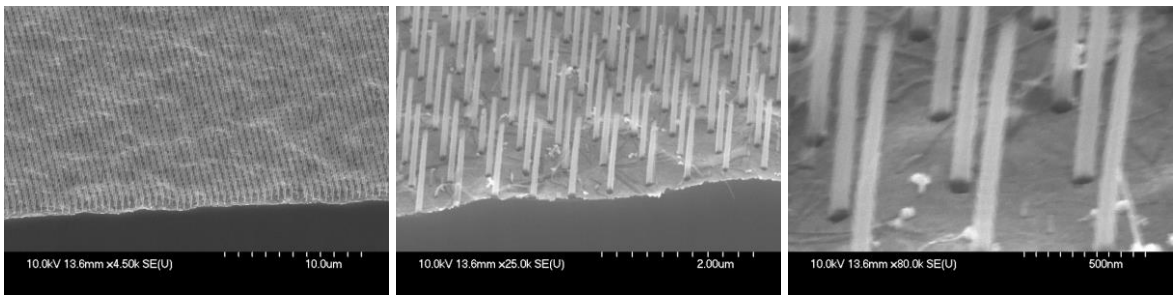


Fig. 7-11: Nanowires from E-beam patterning

7.2.4. Nanosphere Lithography (NSL) followed by MACE

In order to get nanowires of controlled density and diameter, one of the simpler low-cost method is to use nano-sphere colloidal-assembly-based patterning, also known as Nanosphere Lithography (NSL) followed by MACE as illustrated in Fig. 7-12a-h. A simpler alternative was also envisaged for continuous synthesis of nanowires. This process has two main stages:

Stage 1: Nano-sphere colloidal-assembly-based metal patterning (Temperature Assisted Dip Coating for Large-area Assembly of Silica Spheres)

Stage 2: Metal Assisted Chemical Etching (MACE)

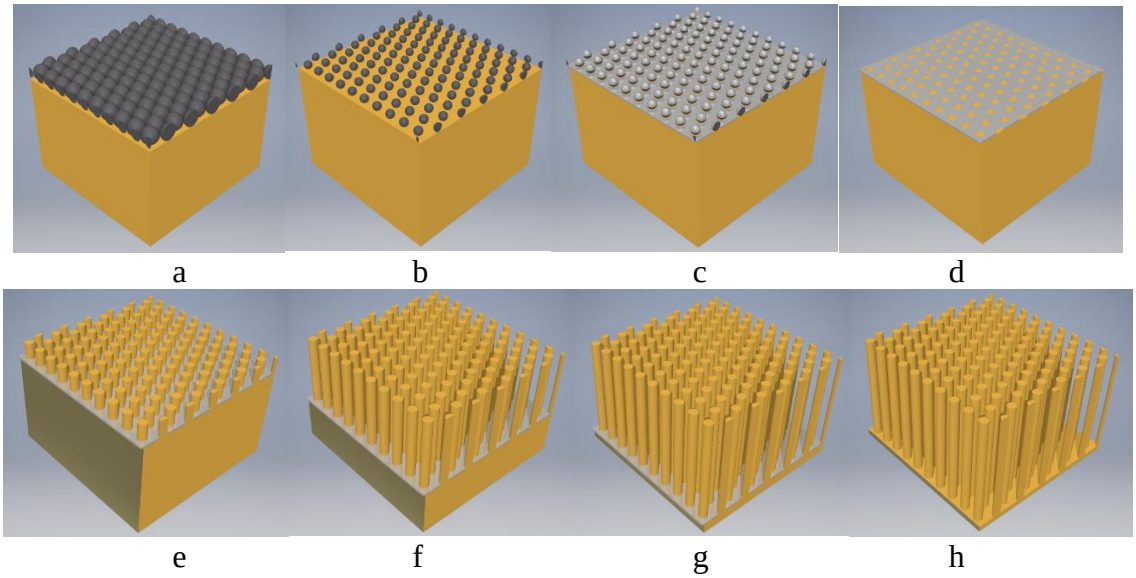


Fig. 7-12: Micro/nanosphere colloidal assembly followed by MACE for fabricating silicon nanowires with controlled density and diameter.(a) 2D close-packed assembly of silica spheres followed by sintering at 650ºC for 10 Minutes (b) RIE for shrinking nanospheres, (c) Silver or Gold deposition followed by (d) removal of silica spheres by ultrasonication, (e-g) Metal Assisted Chemical Etching (MACE) (h) metal removal

As shown in Fig. 7-12(a), 2D close-packed assembly of silica spheres was fabricated followed by sintering at 650ºC for 10 Minutes in order to fix the close-packed assembly. This initial dimension of the spheres will determine the pitch of the nano-mesh. The assembly has been carried out through a temperature assisted dip coating process the setup explained in chapter 3 section 3.1.5 and also published in [27]. Followed by the assembly, RIE was carried out in order to shrink the nanospheres to desired dimension Fig. 7-12(b). This determines the diameter of the Si nanowires. This is followed by silver or gold deposition (Fig. 7-12c) by thermal evaporation. Then the spheres were lifted-off as shown in Fig. 7-12d by ultrasonication, resulting in the formation of nano-mesh Fig. 7-12(e-g) illustrates Metal Assisted Chemical Etching (MACE) process where the etching solution and duration determines the final length of the nanowires. Once the nanowires are formed, the metal was removed (Fig. 7-12h) by etching in solution such as aqua regia.

7.2.4.1. Silica Spheres Suspension

Aqueous monodisperse SiO_2 SPs with average diameters of 100 nm, 500 nm and 1 μm, and standard deviation (SD) of 5, 13 and 26 nm, respectively, and a SPs weight concentration (w/v) of 5% (from Microspheres-Nanospheres) have been used in this work. Stability of the suspension with time plays a critical role in the performance of dip coating. UV-Vis-NIR transmission spectroscopy has been used to characterize SPs of various concentration and with time. Transmittance (T) of suspensions with various w/v has been measured over time (Fig. 7-13). Initial w/v has been diluted by adding different volumes of deionised (DI) water –obtained from a reserve osmosis system (Elix)– resulting in SPs suspension with w/v of 2.5, 1.25, 0.63 and 0.31%. Fig. 7-13 shows T of SPs suspension measured by ultraviolet/visible (UV/Vis/NIR) spectrophotometry (UV2600 Shimadzu) at wavelengths (λ) ranged between 200 and 1300 nm. For the sake of clarity, baseline corresponding to the T of DI water, i.e. w/v of 0%, is also included in Fig. 7-13(a). Prior to the optical characterisation, each suspension is sonicated for 5 min using a probe sonicator from CamSonix, resulting in a stable suspension with high uniform distribution of SPs along the

entire suspension volume. This trend is further confirmed in the inset of Fig. 7-13(a), where T –measured e.g. at λ of 1144 nm– is represented as a function of SPs w/v.

The stability of a 0.5 μm SPs suspension with a w/v of 5% has been characterised by measuring its transmittance spectrum overtime. Fig. 7-13(b) shows spectral T for λ ranging between 200 and 1300 nm (Inset: enlarged view of spectrum with λ between 925 and 1050 nm) measured over time. From this figure, it can be observed that the SPs suspension is stable over time, exhibiting a low variation of T, i.e. ΔT below 2.5% up to 6 h (see inset of Fig. 7-13(b)). Inset of Fig. 7-13(b) also includes the expression used to calculate ΔT.

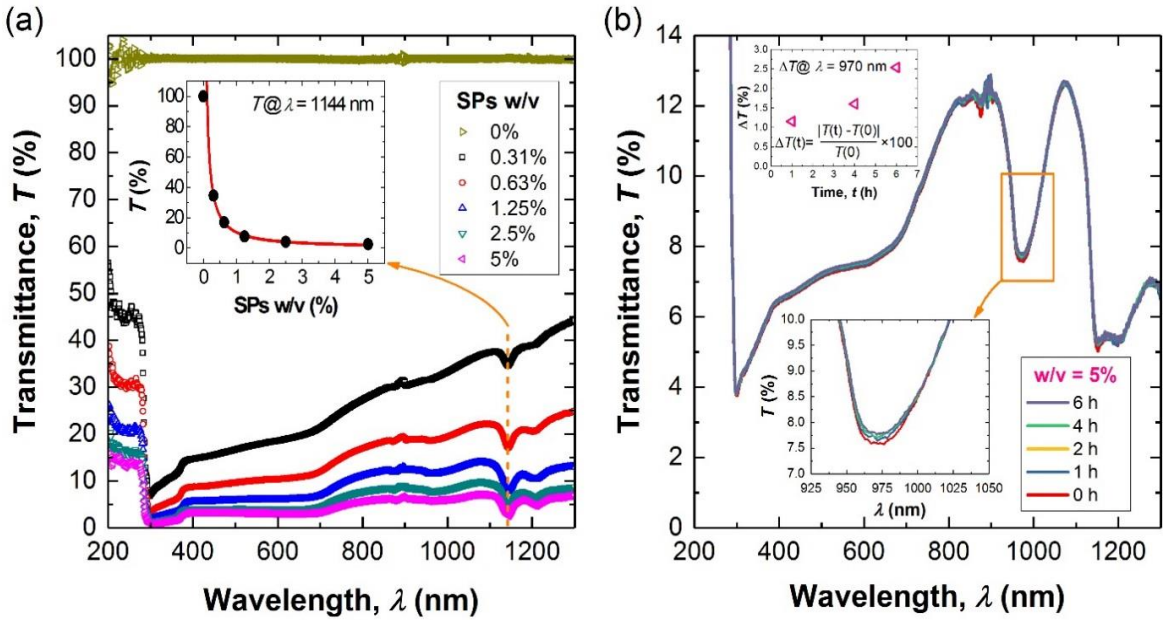


Fig. 7-13: Optical transmittance (T) of 0.5 μm SPs suspension. (a) T vs λ for different SPs w/v%; inset: experimental data and fitting of T vs SPs w/v% @ λ = 1144 nm. (b) T vs λ measured overtime @ w/v of 5%; inset: ΔT overtime @ λ = 970 nm. [27] Carried out in collaboration with CGN, FL, DS, RD. Reprinted with permission from ACS Appl. Mater. Interfaces, 10 (3), 2018. Copyright 2018 American Chemical Society.

7.2.4.2. Receiver Substrate Preparation

The 1.5×1.5 cm^2 pieces of prime grade and single side polished p-type <100> Si wafers, with roughness below 1.5 nm, and resistivity of 1-10 Ωcm, was used as the receiver substrates for dip-coating. Prior to the dip-coating process, native oxide was removed from Si surface by dipping the samples in a low-concentrated HF oxide-etch solution (5:1 buffered oxide etchant, which gives an etching rate of 100 nm/min). After 2 min of HF etching process, the substrate was thoroughly rinsed with DI water and dried under N_2 flow. Thereafter, the substrate was immersed in a piranha solution (H_2SO_4:H_2O_2 in volume ratio of 3:1) for 10 min to remove any organic surface contaminants and to make the surface highly hydrophilic. Again, the substrate is thoroughly rinsed with DI water and dried under N_2 flow. Finally, the substrate is exposed to an O_2 plasma (Oxygen Barrel Asher) at 150 W, using 25 sccm O_2 flux for 4 min to hydroxylate the surface of Si, i.e. to create a uniform coverage of -OH group over the entire Si substrate surface. The contact angle measurements demonstrate hydrophobicity (see **Figure 7-17**(a) of [27]) and hydrophilicity (see **Figure 7-17**(b) of [27]) of Si substrates after HF and O_2 plasma treatments, respectively.

7.2.4.3. Coating Characterisation

In order to achieve assembly of nanospheres and for subsequent use in synthesis of nanowires, a temperature assisted dip assembly setup has been developed, as schematically shown in Fig. 3-10 and explained in chapter 3 section 3.1.5.

After dip-coating, morphological analysis of the SPs coating has been carried out by optical microscopy and scanning electron microscopy (SEM). Optical micrographs are acquired by a digital camera (Leica MC170 HD), using a Nikon optical microscope in reflection mode (objective magnifications ×50 and ×1000). Optical microscopy allows to determine the total surface coverage, and the surface covered by either SPs single layer (SL), SPs multi-layer (ML) or non-assembled SPs. This analysis has been carried out at multiple areas along the coated surface (see **Figure S-2** of [27]). The confirmation of each type of coating is demonstrated by SEM. SEM of SPs coatings is performed with a Hitachi S4700 at following operating parameters: 5 kV and 7.4 mm WD. To improve the sample conductivity, an 80-100 Å thin layer of Au is sputtered onto the SPs coated surface.

7.2.4.4. Experimental Results of Dip Coating

Once the substrate is dipped in the SPs suspension, the liquid solvent adheres to the solid substrate surface due to the intermolecular forces between the solvent and hydroxylated Si surface. The capillarity effect pulled the liquid up forming a concave meniscus. The curvature of the meniscus can be described by the contact angle (θ_m) and the radius of curvature (r_{curve}), and depends on the hydrophilicity of the substrate surface (see **Figure S-3** of [27]). Analysing *in-situ* the dynamic assembly of SPs on Si substrate during dip-coating experiments carried out at above conditions, we noted the formation of three areas, namely: i) deposition area, ii) assembling area, and iii) collection area as schematically illustrated in the inset of Fig. 3-10(b). The deposition area is a dry region where SPs are attached to the receiver substrate, forming either hexagonal close-compact packed (HCP) crystalline structures with different thickness (SL or ML), or a random dispersion of SPs. In the assembling area, SPs adopt almost the final structure but still are embedded in thin film of solvent, which tends to evaporate at a rate J_E which is mainly function of T_s. The solvent evaporation leads to downshift the interface formed between deposition and interface areas, at a speed namely V_m (expressed in μm/s), which depends on T_s as will show later on and. Finally, the collection area is a region of the suspension where volumetric density of SPs is higher with respect to the rest of the suspension due to the continuous flux of particles (J_p) produced by the convective forces in the suspension (J_s). The ratio of substrate surface dip-coated by SL, ML and randomly dispersed SPs is analysed as a function of dip-coating conditions, including T_s, V_w, V_m, θ_w and L_w, as well as the SPs diameter, aiming to find the optimum conditions to dip-coat SiO_2 SPs over large-areas for different applications. For the sake of comparison, outcomes obtained from the analysis are summarised in **Table 19**.

7.2.4.4.1. Effect of Suspension Temperature on Dip-coating

Using 1 μm SiO_2 SPs suspension with a SPs concentration of 0.31% w/v, the surface coverage (ϕ) on a 1.5×1.5 cm^2 Si substrate has been analysed by optical microscopy and SEM as a function of T_s. For these experiments, T_s ranging between RT and 80°C have been studied. Keeping the sample completely immersed in the suspension and at a static position, i.e. $V_w = 0$, the evaporation of the solvent (J_E) leads to downshift the meniscus level at a speed of $V_m>0$, which depends on T_s (Fig. 7-14(a)).

Table 19: Surface coverages of single layer (ϕ_{SL}), multi-layer (ϕ_{ML}) or non-assembled SPs (ϕ_{SPs}) obtained at $V_w = 0$. In brackets, ϕ corresponding to $V_w = V_m$.

ϕ_{SL} (%)	ϕ_{ML} (%)	ϕ_{SPs} (%)	ϕ_T (%)	V_w (μm/s)
10.1 (56.7) ±0.1	0 (0)	23.9 (0) ±0.1	34.0 (56.7) ±0.2	0.37
18.8 (56.2) ±0.2	10.9 (21.6) ±0.2	18.8 (0) ±0.1	48.6 (77.9) ±0.1	0.64
80.9 (100) ±0.1	19.1 (0) ±0.3	0 (0)	100.0 (100) ±0.3	1.30
67.2 (97.9) ±0.1	15.0 (0.5) ±0.1	0 (0)	82.2 (98.4) ±0.1	2.32

At RT, the optical microscopic analysis shows only SPs dispersed randomly over the Si substrate surface, i.e. without forming a continuous close-compact layer of SPs. The lack of T_s strongly reduces V_m which results in a wide meniscus shape, i.e. high r_{curve} and θ_m (**Figure S-3**(a) of [27]), reducing J_s and then J_p towards the collective area. The low density of SPs at the collection area are the main factor hindering the formation of a SPs SAM at RT. Under the described static conditions, i.e. $V_w = 0$, the formation of a close-compact SL and ML of SPs has been observed for T_s above 50°C (Fig. 7-14(a)). This result indicates that the assembly of SPs forming close-compact crystalline structures is clearly influenced by T_s. For $T_s \geq 50$°C, we observed the assembly of SiO_2 SPs forming SL, ML and random dispersions over the surface of Si substrate. At $T_s = 50$°C, the substrate surface is mainly not covered, reaching a total surface coverage (ϕ_T) values of only 34%, with only a small area around ϕ_{SL} = 10.1% covered by a SL (ML formation has not been observed), and the rest of the area (~23.9%) covered by randomly dispersed SPs (ϕ_{SPs}). At $T_s = 60$°C, the ϕ_T increases up to 48.6%, exhibiting also a slight increase of the SL coverage (ϕ_{SL} = 18.8%), the formation of a continuous ML covering around ϕ_{ML} = 10.9% of the whole area, and a decrease of ϕ_{SPs} down to 18.8%. A higher magnification view of the interface formed between SL and ML is presented in the inset of Fig. 7-14(a) where a SEM image taken at that interface shows the clear contrast formed between both regions. The increase of T_s up to 70°C leads to a significant improvement of the ϕ_T, reaching almost 100% coverage of 1.5×1.5 cm^2 total sample area. In these conditions, ϕ_{SL} and ϕ_{ML} reach values of 80.9% and 19.1%, respectively. However, we observed that a further increase of T_s up to 80°C hinders the performance of dip-coating by exhibiting a reduction of the ϕ_T, ϕ_{SL}, ϕ_{ML} down to 82.2%, 67.2%, and 15.0%, respectively. This reduction of ϕ_{SL} and ϕ_{ML} is occurring because of the non-assembled SPs (ϕ_{SPs}) as observed in Fig. 7-14(a). **Table 19** summarises ϕ_T, ϕ_{SL}, ϕ_{ML} and ϕ_{SPs} as a function of T_s, excluding the RT conditions (which may not be relevant for this discussion). Standard error of the mean data recorded in **Table 19**, corresponding to a series of at least five experiments performed at each condition. The low dispersion of the obtained ϕ (< ±0.3) confirms the reproducibility of the developed procedure.

The above results prove that T_s has a strong influence on the assembly of SPs on a hydroxylated Si surface (which has a direct effect on ϕ_T) and on the self-assembly process as demonstrated by the formation of both SL and ML. In this regard, we hypothesize that the increase of T_s leads to the change of the meniscus shape, reducing both θ_m and r_{curve} the intermolecular forces act on the solvent adhered to the substrate surface, elongating the meniscus, and then, reducing both θ_m and r_{curve} (**Figure S3**(b) of [27]). This effect is expected to be larger as T_s increases. For the sake of explanation, one can define V_s and V_m, as the

downshift speed of the suspension level and meniscus level, respectively, allowing to study the speed of the top part of the meniscus (V_m) which can be different than the total solution level mainly due to the capilarity effect (V_s). The increase of T_s leads to an increase of both V_s and V_m, however, due to a large area exposed to the air, V_s - V_m is expected to be always positive. As the difference between V_s and V_m increases with T_s, the height of the liquid column adhered to the substrate surface increases. In this scenario, the gravity force reduces both θ_m and r_{curve} (see **Figure S-3**(b) of [27]), which can contribute to the increase of the SPs flux towards the collection area (J_p).[232,269] However, an excess of temperature (T_s >80°C) could lead to the deposition of SPs ML at expense of SL (T_s = 80°C in Fig. 7-14(a)), mainly due to the accumulation of high density of SPs at the collection area. On the other hand, the less temperature (T_s < 50°C in Fig. 7-14(a)) hinders the formation of SiO_2 SPs SL and ML mainly due to the low concentration of SiO_2 SPs at the drying region. All these factors lead to the formation of periodic stripes of SL and ML and reduce ϕ_{SPs} and non-covered areas, which are in good agreement with previous observations.[232,269] In order to prevent the formation of stripes, and to obtain the deposition of a continuous SPs SL, the use of different withdrawal speeds is investigated in this work.

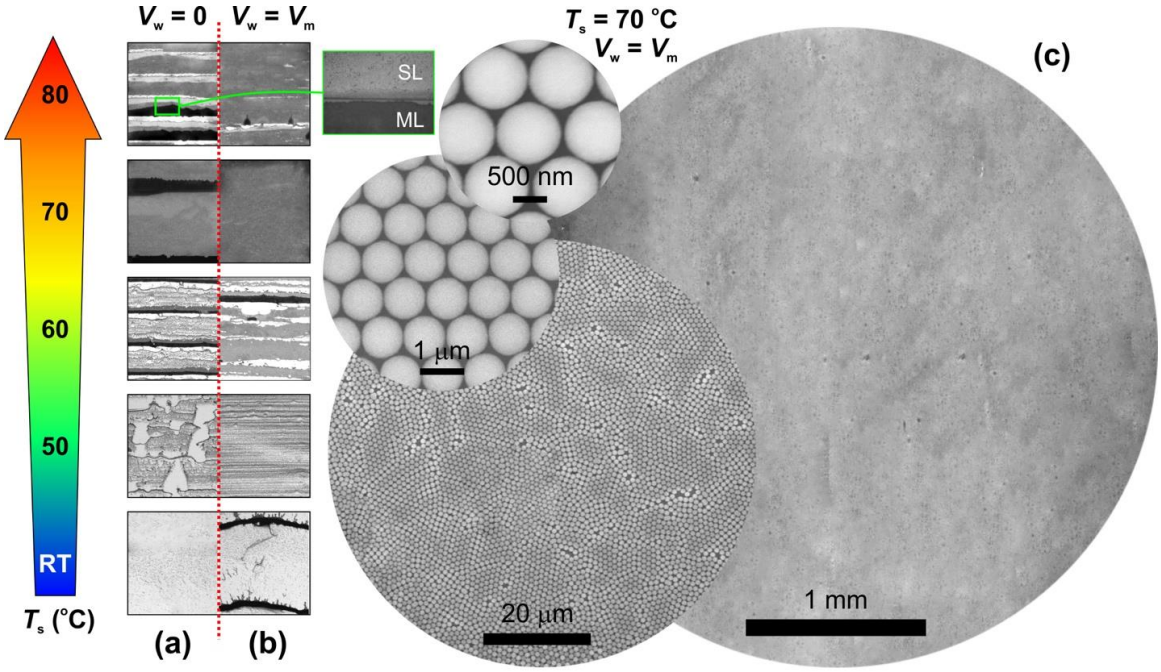


Fig. 7-14: Optical characterisation of 1 μm SiO_2 SPs dip-coated on 1.5×1.5 cm^2 Si substrates at RT < T_s < 80 °C using V_w of (a) 0 and (b) V_m. Inset: SEM image of SL/ML interface. (c) SEM images of SiO_2 SPs SAM formed at 70 °C and V_w of V_m. [27] Carried out in collaboration with CGN, FL, DS, RD. Reprinted with permission from ACS Appl. Mater. Interfaces, 10 (3), 2018. Copyright 2018 American Chemical Society.

7.2.4.4.2. Effect of Withdrawal Speed on Dip-coating

It is clear that a simple evaporation of solvent can form SL of SiO_2 SPs on a hydroxylated Si substrate surface at T_s > 50°C. We further investigate the effect of speed of substrate withdrawal on ϕ. For initial V_w we chose to use a speed similar to V_m because we hypothesize that synchronising both speeds would improve the formation of SPs SAM, i.e. increasing ϕ_T *and* ϕ_{SL} while reducing both ϕ_{ML} and ϕ_{SPs}. The V_w was in the range of 0.1-100 μm/s, which

is similar to those reported in the literature for dip-coating of large SiO_2 SPs SAM.[270,232] However, in those experiments the role of J_E (and associated T_s, RH and V_m) was not clearly established. Here, we have experimentally determined the V_m in SPs suspensions (SPs diameter of 1 μm and SPs concentration of 0.31% w/v) as a function of T_s, using an optical microscope and a micrometric scale to measure the shift of the meniscus top-part overtime. These values are mentioned in the last column of **Table 19**. A series of dip-coating experiments were carried out at T_s of 50, 60, 70 and 80°C, using a V_w of 0.37, 0.64, 1.30 and 2.32 μm/s, respectively to obtain V_m at each T_s. The range of V_w used here is 3 orders of magnitude slower than that used by Wang et al.[270] for the room-temperature dip-coating of 2 μm SiO_2 SPs over record-breaking large areas (~0.3 cm^2). However, as we demonstrate that the chosen range of V_w dramatically improves the surface coverage of SPs SAM under temperature-assisted dip-coating conditions.

Comparing the performance of dip-coating processes carried out at $V_w = 0$ (Fig. 7-14(a)) and $V_w \neq 0$ (Fig. 7-14(b)) we note that the latter clearly shows positive effects on the assembly of SiO_2 SPs at large areas. In the case of RT, we observe an improvement in the ϕ_T reaching values around 23% mainly because the formation of both SL and ML, as well as the attachment of non-assembled SPs. In this case, the solvent evaporation occurs after the whole substrate is outside the SPs suspension. This leads to the formation of evaporation regions with random shapes, i.e. the deposition interface is not flat as observed in dip-coatings carried out at higher temperatures, promoting the uncontrolled accumulation of SPs at the boundaries of the evaporation regions, resulting in the formation of ML rather than SL. At T_s = 50°C and V_w = 0.37 μm/s, the increase of ϕ_T and ϕ_{SL} up to 56.7% (from 34.0% obtained at $V_w = 0$) and 56.7% (from 10.1% obtained at $V_w = 0$), respectively is noted while hindering the attachment of non-assembled SPs, i.e. ϕ_{SPs} ~0. In addition, we observe an improvement in the coverage uniformity over the 1.5×1.5 cm^2 analysed area (Fig. 7-14(b)). At T_s = 60°C, the use of a V_w = 0.64 μm/s reduces ϕ_{ML} down to 21.6%, while showing similar ϕ_{SL} of 56.2%. This means there is a slight enhancement of the ϕ_T up to 77.9% with respect to the static conditions (48.6% at $V_w = 0$). On the other hand, we observe that using T_s = 70°C and V_w = 1.3 μm/s, both ϕ_T and ϕ_{SL} are enhanced and reach values closer to 100% of 1.5×1.5 cm^2 area, whereas the contribution of ML is almost negligible (ϕ_{ML}~0). In contrast, a further increase of the temperature up to T_s = 80°C and using a higher V_w = 2.32 μm/s, results in a high ϕ_T of 98.4%, but showing the formation of small areas consisting of SPs ML (ϕ_{ML} = 0.5%). Last result confirms that the use of an extremely high T_s, even at dynamic conditions ($V_w > 0$), hinder the formation of SPs SL mainly because: i) the J_p increases at the collection area, and ii) the increase of J_E expands the evaporation area and promotes the formation of ML rather than SL.

Analysing ϕ, the withdrawal of the sample at V_w in the range of V_m has been demonstrated to produce an increase of both ϕ_T and ϕ_{SL}. This result proves that V_w of 1.30 μm/s is a "natural" assembling speed (V_{w0}) at T_s = 70°C for 1 μm SiO_2 SPs and the ambient RT and RH of 20%. To demonstrate this, we further analysed the surface morphology of 1.5×1.5 cm^2 Si substrate dip-coated at T_s = 70°C and using V_w below and above V_{w0} = 1.30 μm/s. The former conditions i.e. $V_w < V_{w0}$ show results similar to those presented in Fig. 7-14(a) for T_s = 70°C, where V_m predominant over V_w promotes the formation of ML and results in a periodic SL and ML stripes. On the other hand, at $V_w > V_{w0}$ we observed a uniform coverage of SPs clusters consisting 2-10 SPs uniformly covering the whole substrate area. These results are in good agreement with previous works,[232] where dip-coating

experiments (carried out in similar conditions and using SPs with diameters ranged between 0.21-2.1 μm) conclude that there is a characteristic transition V_w around 2.3 μm/s above what the formation of narrow stripe-like patterns is promoted, and below what the deposition of a continuous SPs SAM can be obtained. In this work, we present for the first time the natural assembling speed for SiO_2 SPs, below the transition V_w,[232] that allows the deposition of SAM over record-breaking large areas around 1.5×1.5 cm^2.

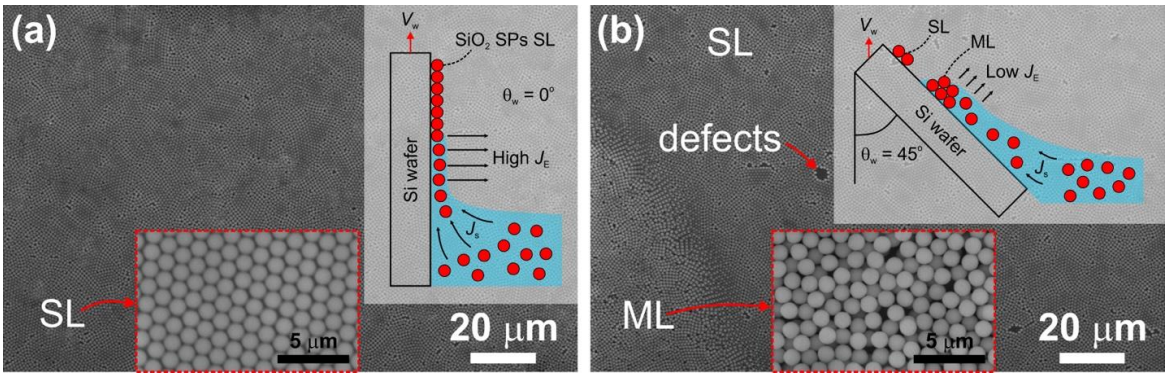


Fig. 7-15: SEM images of dip-coating experiments carried out at θ_w of (a) 0° and (b) 45°. Insets: 2D schematic illustrations of the dip-coating conditions (top-right), higher magnification SEM images of SL and ML regions (bottom). [27] Carried out in collaboration with CGN, FL, DS, RD. Reprinted with permission from ACS Appl. Mater. Interfaces, 10 (3), 2018. Copyright 2018 American Chemical Society.

7.2.4.4.3. Effect of Withdrawal Angle on Dip-coating

The gravity has been demonstrated to play a major role in the SPs assembly by dip-coating method mainly because it directly affects curvature of the meniscus. Dip-coating experiments are carried out through vertical withdrawal of the receiver substrate from the SPs solution.[232,270] Here, we have compared the performance of dip-coating experiments carried out at different withdrawal angles, including θ_w = 0° (Fig. 7-15(a)) and 45° (Fig. 7-15(b)), where θ_w is defined as the angle formed between the sample surface and the withdrawal direction (see insets of Fig. 7-15). For these experiments, we have used a T_s = 70°C and V_w = 1.3 μm/s and SPs with a diameter of 1 μm. Fig. 7-15(a) and (b) show the SEM images of representative areas of samples dip-coated at θ_w of 0° and 45°, respectively. From these figures, one can deduce that θ_w has an important role on the SPs assembly, θ_w of 0° shows better results in terms of large areas coating of SPs SL (see SAM of SiO_2 SPs in the bottom inset of Fig. 7-15(a)). In contrast, the at θ_w = 45° the formation of defects (i.e. empty areas where SPs are not forming close compact structures) is prominent along with MLs consisting of vertical stacked SPs as highlighted in the bottom inset of Fig. 7-15(b). This behavior can be explained due to local defects existing along the area of the receiver substrate (possibly created during the substrate preparation), which may lead to a local variation of the wettability along the substrate area, causing the formation of a non-flat deposition interface in the top part of the meniscus. As illustrated in the insets of Fig. 7-15(a, b), the increase of θ_w increases the thickness of the meniscus and this leads to reduced convective flow of SPs towards the evaporation area (low J_p and J_s) and reduces J_E. These both hinder the formation of a continuous SL, while promoting the formation of defects and locally MLs. In contrast, the reduction of θ_w down to 0° decreases the thickness of the meniscus and increases J_E, J_p and J_s which improve the formation of large area SL while lowering the chances of the formation of defects and ML (Fig. 7-15(a)).

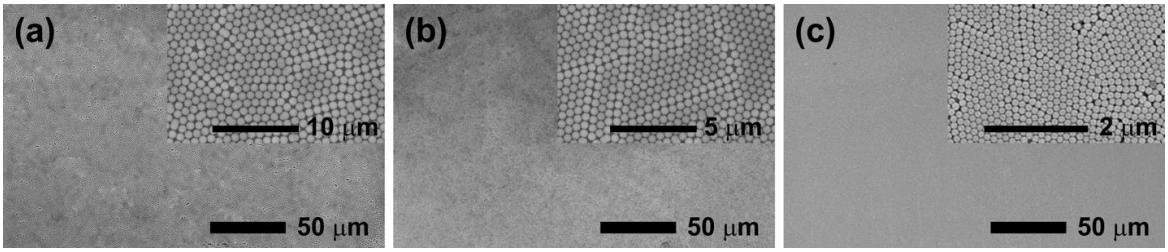


Fig. 7-16: SEM images of Si substrate surface dip-coated with SiO_2 SPs of different diameters, comprising (a) 1 μm, (b) 500 nm, and (c) 100 nm, using T_s = 70ºC, V_w = 1.3 μm/s and a suspension concentration of 0.31% w/v. Insets: higher magnified SEM images of SiO_2 SLs. [27] Carried out in collaboration with CGN, FL, DS, RD. Reprinted with permission from ACS Appl. Mater. Interfaces, 10 (3), 2018. Copyright 2018 American Chemical Society.

7.2.4.4.4. Effect of SPs Diameter on Dip-coating

Dip-coating of SPs with diameters ranged between 200 nm to 2 μm has been reported in literature.[270,271] Here we present an investigation of the effect of SPs size on the dip-coating assembly mechanism including the dip-coating of nanometric SiO_2 SPs (diameter of 100 nm) and in this regard the results in this section are complementary to the previous works. The large-area dip-coating of SPs with different diameters, including 1 μm, 500 nm and 100 nm is thoroughly analysed here for applications that will be presented in the next section. For the sake of comparison, we have used the same suspension concentration of 0.31% w/v independently of the SPs size, and standard dip-coating experimental conditions, i.e. T_s = 70ºC, V_w = 1.3 μm/s and θ_w = 0º. Fig. 7-16 presents SEM images of resulting Si substrate surface morphology after dip-coating experiments carried out using SiO_2 SPs with diameters 1 μm (Fig. 7-16(a)), 500 nm (Fig. 7-16(b)) and 100 nm (Fig. 7-16(c)). From those figures, one can observe that there is: i) a good SL coverage uniformity (100% surface coverage), ii) low defects density, iii) HCP crystalline structure, and iv) absence of ML and non-assembled SPs regions. Analysing areas dip-coated by a similar number of SPs (see insets of Fig. 7-16), it is observed that statistically the defects are more or less independent of the SPs diameter. Figure S-4 in supporting information shows assembly of the resulting SLs for similar areas dip-coated with SPs of different diameters. The crystallinity of the assembly can be improved by carrying out the process with highly mono-dispersed SPs. As clearly observed in the inset of Fig. 7-16(c), by reducing the size of the SPs down to diameters of 100 nm, dip-coating produces grain boundaries between regions with hexagonal close compact structures. From this figure, one can roughly estimate that grains have an average size of around 1 μm^2. Considering a HCP structure, the area covered by a single cell (consisting in 6 SPs) of SPs with a diameter of 100, 500, and 1000 nm is 2.4×10^{-10}, 5.8×10^{-9}, and 1.5×10^{-8} cm^2, respectively. Accordingly, the SAM domain size decreases with the SPs diameter, making more difficult to obtain single domain SAM as the SPs size reduces. The achievement of single domain SAM, preventing the formation of grain boundaries (see inset of Fig. 7-16(c)) could strongly affect the performance of SPs coatings for applications such as those presented in this work (see section 7.3.2). In addition, the huge areal extension obtained with nanometric SiO_2 SPs (diameter of 100 nm) makes the temperature-assisted dip-coating approach presented here, an excellent alternative for the deposition of highly ordered and compact nano-SPs over large areas (Table 1 of [27]).

7.2.4.5. MACE followed by NSL

Fig. 7-17(a) shows the effect of sample pre-treatment on the hydrophilicity of the surface. The contact angle of bare silicon wafer was 64^0. After plasma O_2 treatment of sample at 100 Watt for 5 mins the sample become highly hydrophilic resulting in a very high contact angle as shown in Fig. 7-17b. Fig. 7-17(c) and Fig. 7-17(d) shows large area assembly of 1 µm and 100 nm silica spheres using the proposed method. Fig. 7-18 presents a 3D schematic illustration of MACE fundamental steps, comprising of: (a) dip-coating of SiO_2 SPs over a large-area Si wafer surface (with native oxide); (b) reactive-ion etching (RIE) of SiO_2 SPs using CHF_3/Ar (25 sccm / 18 sccm), 200 Watt, 30 mT at RT for (b1) 0, (b2) 5, (b3) 8, (b4) 11, (b5) 15, and (b6) 17 min; (c) deposition of 100-200 nm of Ag layer (see SEM image in (c1)); (d) sonication in ethanol for 5 min creating a periodic distribution of micro-holes (see SEM image in (d1)); (e) MACE process dipping the sample in a HF:H_2O_2 solution for 30 min resulting in vertically aligned Si NWs (see SEM image in (e1)).

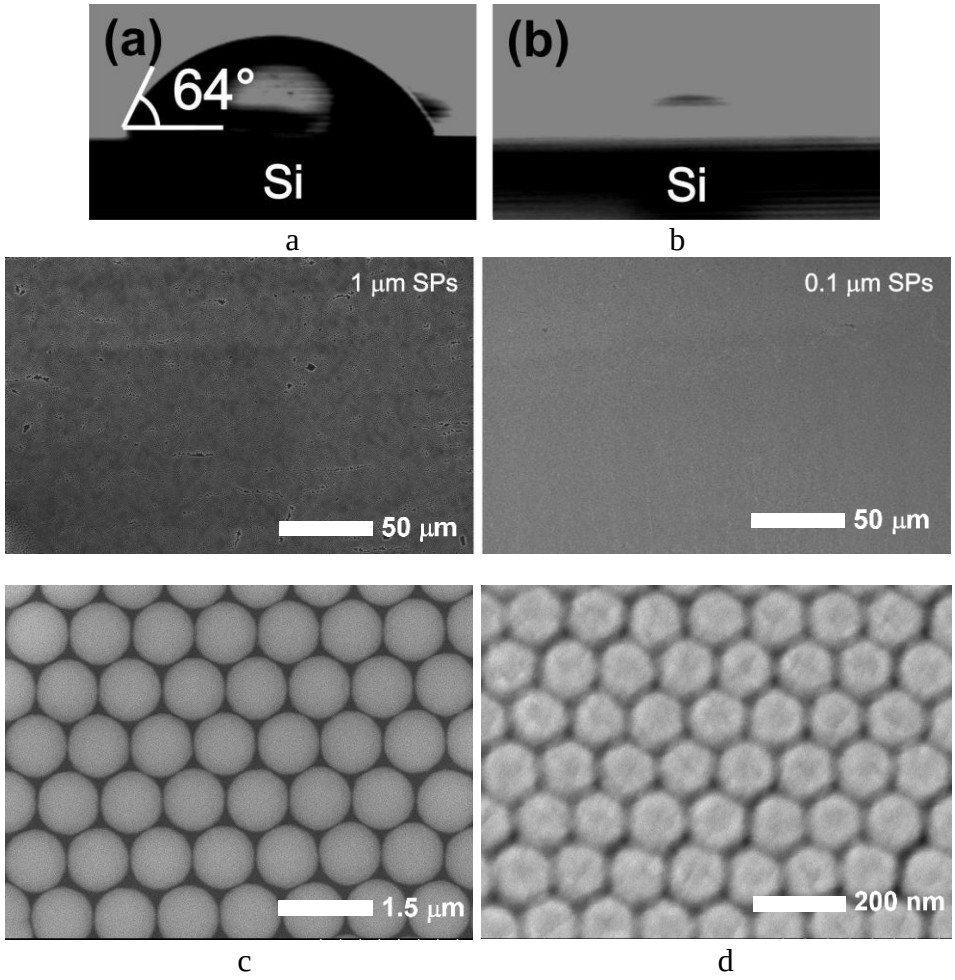


Fig. 7-17: Effect of sample pre-treatment on hydrophilicity before dip coating(a)Bare Si wafer and (b) hydroxylated Si surface. Large area assembly of (c) 1µm spheres and (d)130 nm spheres. [27] [27] Carried out in collaboration with CGN, FL, DS, RD. Reprinted with permission from ACS Appl. Mater. Interfaces, 10 (3), 2018. Copyright 2018 American Chemical Society.

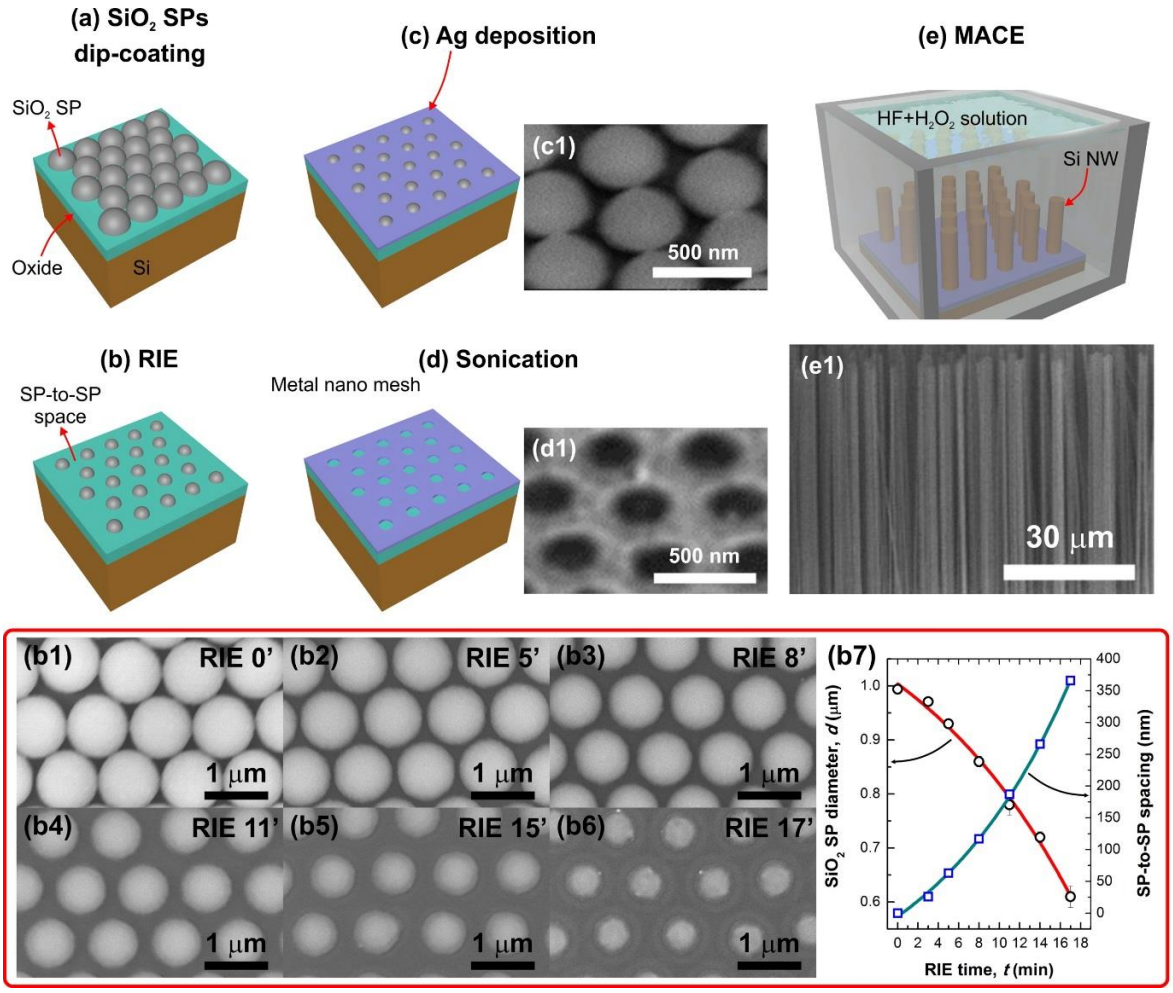


Fig. 7-18: 3D schematic illustration of MACE steps for the synthesis of Si NWs, comprising of: (a) dip-coating of SiO2 SPs over a large-area Si wafer surface (with native oxide); (b) reactive-ion etching (RIE) of SiO2 SPs using CHF3/Ar (25 sccm / 18 sccm), 200 Watt, 30 mT at RT for (b1) 0, (b2) 5, (b3) 8, (b4) 11, (b5) 15, and (b6) 17 min; (b7) SPs size and SP-to-SP spacing vs RIE time; (c) deposition of 100-200 nm of Ag layer (see SEM image in (c1)); (d) sonication in isopropanol for 5 min creating a periodic metallic nano mesh (see SEM image in (d1)); (e) MACE process dipping the sample in a HF:H2O2 solution for 30 min resulting in vertically aligned Si NWs (see SEM image in (e1)). [27] Carried out in collaboration with CGN, FL, DS, RD. Reprinted with permission from ACS Appl. Mater. Interfaces, 10 (3), 2018. Copyright 2018 American Chemical Society.

Initially, 1 μm SiO_2 SPs are dip-coated on top of a 1.5×1.5 cm^2 Si substrate as schematically depicted in Fig. 7-18(a) and demonstrated by SEM analysis (Fig. 7-18(b1)). Prior to the MACE process, we purposely decrease the initial SPs diameter and increase the SP-to-SP spacing by RIE to achieve NWs with controlled diameter. Resulting SPs diameter and SP-to-SP spacing have been analysed by SEM (Fig. 7-18(b1-b6)). Fig. 7-18(b7) records average SPs diameter and SP-to-SP spacing obtained from SEM analysis and their corresponding standard deviation as a function of the RIE time. This figure includes experimental data obtained from SEM analysis along with the best fitting corresponding to an exponential function. This method permits us to reduce the initial size of the SPs from 1 μm down to 600 nm which has a direct effect on the diameter of resulting NW during MACE. This also offers a simple way to develop NWs with different diameters to meet the

requirements of a target application. Similar RIE process carried out with 500 and 100 nm SPs resulted in continuous SiO_2 SPs SL, comprising SPs diameters from 20 nm to 1 µm. After RIE step, we deposit Ag layer by thermal evaporation. To prevent the formation of a continuous Ag layer on top of the Si substrate its thickness is less the height of assembled SPs Fig. 7-18(c1). The discontinuity of the metallic nano mesh is a key feature that allows the successful development of MACE process.[272] Resulting sample is then dipped in ethanol and sonicated for 5 min to remove the SPs from the substrate surface. Fig. 7-18(d) shows the SEM image of a resulting porous Ag layer after the sonication step. As mentioned above, the pore size can be roughly controlled by the initial size of the SPs. Since the Ag thermal evaporation is highly directional, each SP present a mask over the Si substrate surface, slightly increasing the pore size with respect to the SP diameter. Finally, the sample is dipped in a HF:H_2O_2, promoting the preferential etching of Si wafer underneath the Ag layer, and resulting in vertically-aligned Si NWs on top of Si wafer as demonstrated by SEM Fig. 7-18(e1). The advanced use of temperature-assisted dip-coating method to create periodic SiO_2 SPs SAM stripes over large areas would allow to control the NW-to-NW spacing resulting from MACE. Therefore, this is a promising low-cost and easy-of-developing approach for improving performance e.g. of transfer-printing of NWs over large areas.[273]

7.2.4.6. Challenges with conventional NSL for nanopatterning:

NSL patterning is suitable for realising nanowires above 75 nm. However, there are challenges associated in realising sub-75 nm structures directly from NSL. Fig. 7-19a shows metal mesh of various pore diameters. There is a major challenge in achieving a >15 nm thick porous metal mesh of pore diameter <75 nm reliably using NSL. Fig. 7-19c6 shows a damaged metal mesh during lift off for 70 nm spheres diameter after 6 minutes of bath ultrasonic agitation. The spheres get released only after the film gets damaged in such dimensions.

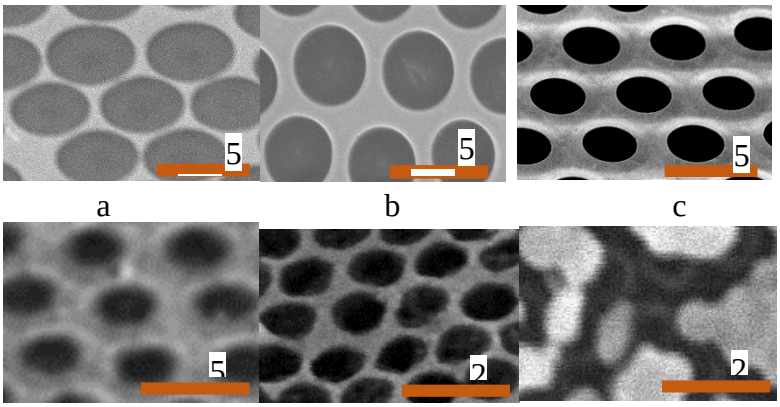


Fig. 7-19: Metal mesh of various pore diameters a: 4.25 µm, b: 3.75 µm, c: 3.5 µm obtained from 4.8 µm spheres and of diameter d: 300 nm obtained from 480 nm spheres e: 90 nm obtained from 130 nm spheres f: Damaged metal mesh during lift off for 70 nm spheres diameter.

In order to overcome this challenge, a modified approach has been proposed to fabricate sub-30 nm nanowires as discussed in the next section. This sub-30 nm nanowires favours efficient JLFETs.

7.2.5. Modified NSL followed by MACE for fabricating sub-30 nm Nanowires

Fabricating nanowires of <100nm using NSL has significant challenge associated with it, as explained in the previous section mainly because of the issue with nano-mesh formation. Recently, Li *et al.* [274] have used MACE followed by thermal oxidation to achieve sub-20 nm nanowires. However, use of high temperature process is undesirable (950^0C up to 60 minutes) and has disadvantages in terms of associated cost and can damage/disturb the crystallinity of the wires. In this regard, here we demonstrate a simple approach for fabricating sub-30nm nanowires using NSL. The approach uses a double metal system where NiCr (60:40) act as a barrier mask while the Gold or Ag acts as a MACE mask. After forming the closed pack assembly of ~100 nm spheres, in contrast to the previous method, instead of doing a RIE to shrink the spheres, NiCr is directly evaporated using a e-beam evaporation system. This results in the formation of sub-30nm patterns between the gaps in closed packed assembly as shown in Fig. 7-20. Lift-off of the spheres with ultrasonic agitation result in leaving behind the hexagonal assembly of sub-30 nm features (Fig. 7-20b). SEM image of typical features are shown in Fig. 7-20c. On top of this, silver or gold film is deposited (Fig. 7-20d) followed by MACE to achieve nanowires of desired height. Fig. 7-20 (d) shows SEM images of sub-30 nm nanowires synthesised using this approach.

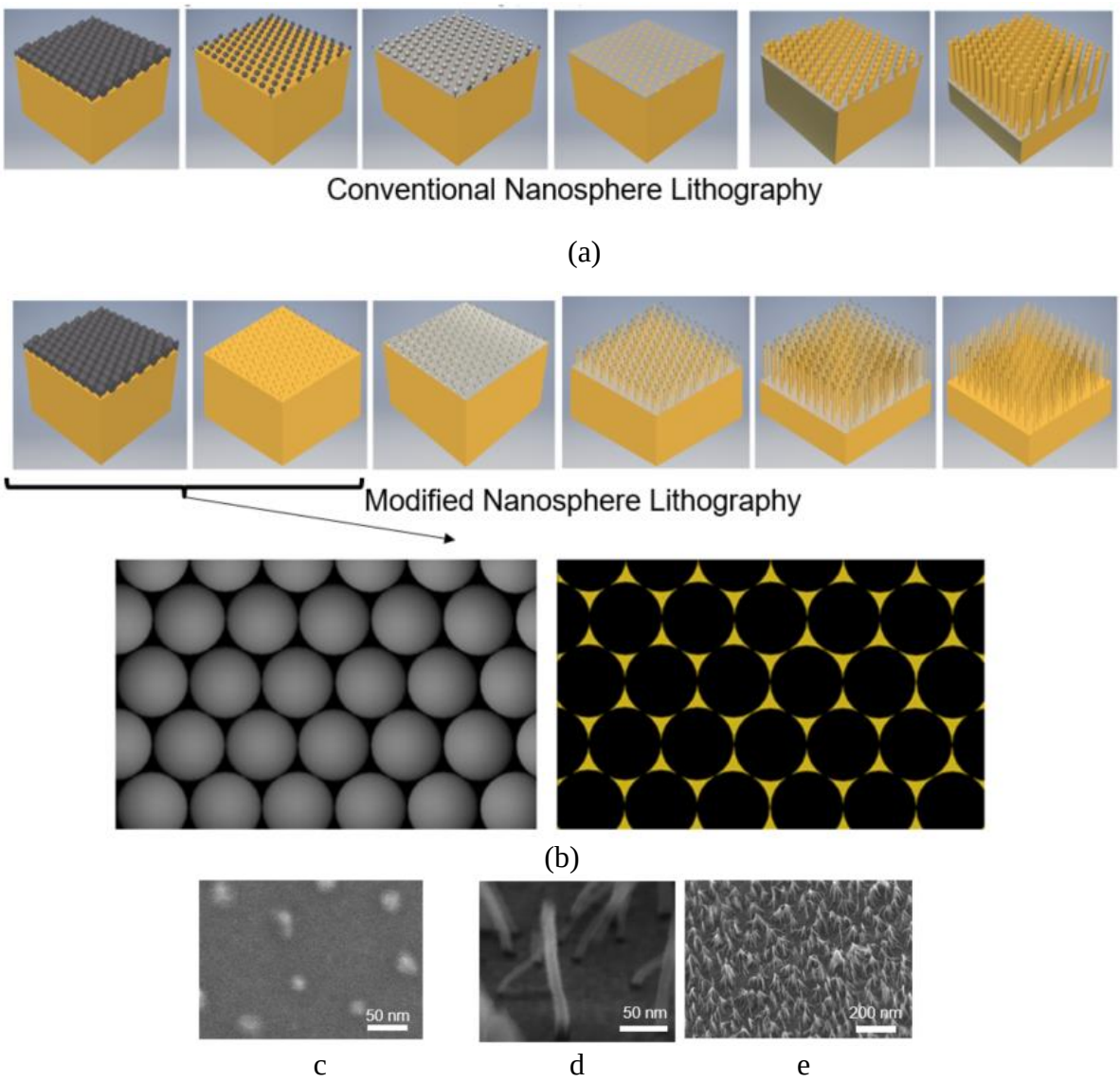
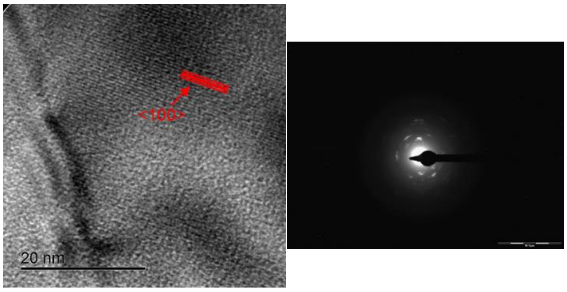


Fig. 7-20: (a) Conventional nanosphere lithography followed by MACE (b) Modified nanosphere lithography followed by MACE (c) nanopatterns (d) Realised sub-30nm nanowires (e)bundling of nanowires

Challenges to overcome with sub-30 nm nanowires:

While with the above approach sub-30 nm nanowires were realised, this method has a problem which must be overcome before realising devices. Mainly as observed in Fig. 80 high aspect ratio sub-30 nm nanowires tend to bundle together when the sample is taken out of the wet solution and dried. This offers problem in the printing of nanowires.

Another problem is the porosity of the resulting wires. TEM imaging was also carried out on the nanowires as explained in section 3.2.1. The crystallinity of the sub-30 nm wires were poor as observed from TEM (Transmission Electron Microscope) images and the associated diffraction pattern. Few crystalline regimes of tens of nanometers diameter are observed in an amorphous matrix. These two problems must be solved for realising electronic devices from the sub-30 nm wires which is a work-in-progress.



a b

Fig. 7-21: (a) TEM image of fabricated sub-30 nm nanowires and (b) associated diffraction pattern for the same sample

7. 3. Printing of Nanowires and Device Fabrication

The next step is to carry out printing of nanowires for realising functional electronics from nanowires as illustrated in Fig. 7-1. Nanowires of diameter >75nm are suitable for contact printing because of lack of bundling. The bundling problem present in nanowires of sub-30nm poses a problem for contact-printing based realisation of devices. The nanowires >75nm diameter are suitable for application as sensor component or as resistive elements. For realising JLFET it is important to have nanowires of sub-30nm diameter. With reference to this, two methods are explored for realising functional electronics from nanowires: 1) Contact printing 2) Large-area DEP based transfer printing.

7.3.1. Contact Printing Experiments

The following section describes a homemade contact-printing system with close-loop control which was used for printing both bottom-up and top-down semiconductor NWs from the growth substrate to defined location on the receiver substrate. The top-down silicon wires were synthesised using MACE process as explained above[29]. The bottom up ZnO nanowires were synthesised using vapour-phase growth as schematically illustrated in section and detailed in [29]. The high reliability and reproducibility achieved by the developed system allows an accurate control over the NW printing process through operational parameters (e.g., contact pressure between donor (NW substrate) and receiver (foreign substrate) substrates and the sliding speed/stroke of the receiver substrate). The NW transfer yield, evaluated from resulting NW density (NWs/μm) and NW-to-NW spacing, has been analysed as a function of the above printing parameters. Finally, contact-printing method has been successfully used to fabricate ultraviolet (UV) photodetectors (PDs) with ZnO and Si NWs multiNW electronic layers—printed in a Wheatstone bridge (WB) configuration—acting as the photosensitive material and electronic component, respectively.

The basics of contact printing involves the directional sliding of a growth substrate (also called donor substrate), consisting of free-standing nanowires (NWs), on top of a receiver substrate. During the sliding step, NWs tend to be aligned and combed due to the sliding shear force. The wires then get detached from the donor substrate due to the accumulation of structural strain, and finally are anchored by the van der Waals interactions with the surface of the receiver substrate, resulting in NWs aligned along the surface of the receiver substrate. The system used for this explained in section 3.1.6.1.

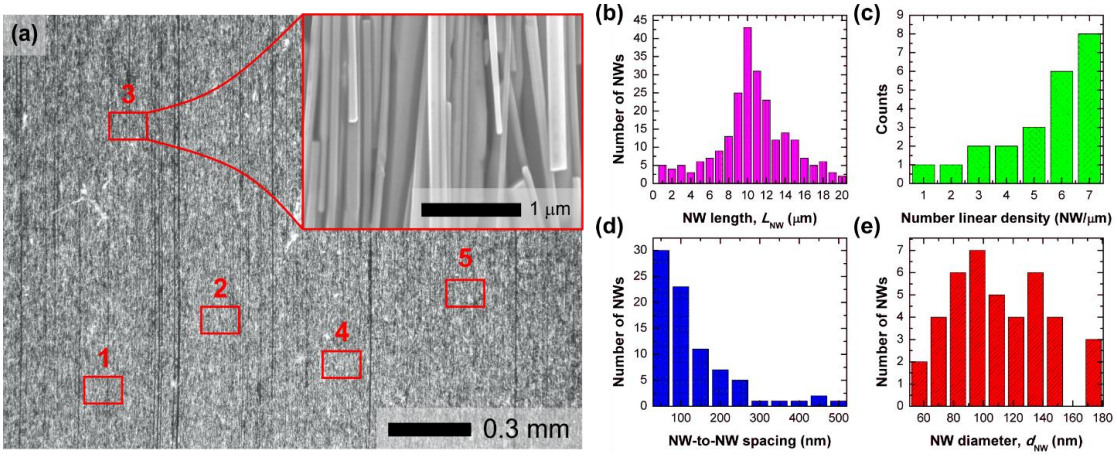


Fig. 7-22: Contact-printing of ZnO NWs. (a) Optical microscopy and (inset) SEM images of ZnO contact-printed on Si(100) substrates. Statistical analysis of contact-printing performance carried out on 5 different areas randomly chosen along the total sample area, analysing (b) NW length, (c) NW linear density (d) NW-to-NW spacing, and (e) NW diameter, along a 10-μm long horizontal profile (see inset of (a)). [233]Carried out in collaboration with CGN, FL, DS. Nature: Microsystems & Nanoengineering, 4, 22 (2018) CC BY 2.0.

The area of an electronic device that needs to be printed by a SAM of NWs is mainly given by its architecture, i.e. the distribution of the electrodes and the position and size of the NWs SAM with respect to the rest of the components. Our contact-printing setup has demonstrated to carry out the high-performance printing of NWs SAM with approximately the same dimensions of the donor substrate, allowing the integration of NWs onto almost every device architecture. We have studied the transfer performance of our system by characterising the morphology of as-printed NWs by means of optical microscopy and SEM, and calculating figure-of-merit such as NW length/diameter, NW linear density (NWs/μm), and NW-to-NW spacing. The dimensions of the donor substrate used in this experiment are around 1×1 cm^2. Since the area contact-printed by NWs is in the range of cm^2, whereas the SAM is based on NWs with a footprint around hundreds of nm, the variation of above parameters along the sample surface could be significant. In order to minimize any potential errors, we have carried out a statistical analysis of different areas for both ZnO NWs (Fig. 7-22) and Si NWs (Fig. 7-23). As an example, Fig. 7-22 and Fig. 7-23 show the analysis carried out here for ZnO and Si NWs, respectively, contact-printed on a Si(100) substrate using a force of 5 N (50 kPa) and a sliding speed of 100 μm/s. For the statistical analysis of the contact-printing performance, up to 5 different areas (insets of Fig. 7-22 and Fig. 7-23), have been randomly chosen along a total area of 1×1 cm^2 (Fig. 7-22(a) and Fig. 7-23(a)). The distribution of NWs size (diameter and length), NW-to-NW spacing, and NW linear density (NWs/μm) are calculated along a 10 μm length horizontal profile drawn in the SEM figure (see insets of Fig. 7-22(a) and Fig. 7-23(a)). From this analysis, one can extract the following information: i) the average length of contact-printed ZnO and Si NWs is around 10 μm (Fig. 7-22(b) and Fig. 7-23(b)), the maximum NW linear density is around 7 NW/μm (ZnO NWs, Fig. 7-22(c)) and 3 NW/μm (Si NWs, Fig. 7-23(c)), the average NW-to-NW spacing is about 50 nm in ZnO and Si NWs (Fig. 7-22(d) and Fig. 7-23(d)), and the average diameter of ZnO and Si NWs is around 95 (Fig. 7-22(e)) and 115 nm (Fig. 7-23(e)), respectively. This is an example of the analysis carried out for contact-printing experiments using above conditions (contact force of 5 N and a sliding speed of 100 μm/s). In the Results and Discussion section, the effect of operational parameters such as contact pressure and

sliding speed on the contact-printing performance is analysed similar to the results presented in Fig. 7-22 and Fig. 7-23.

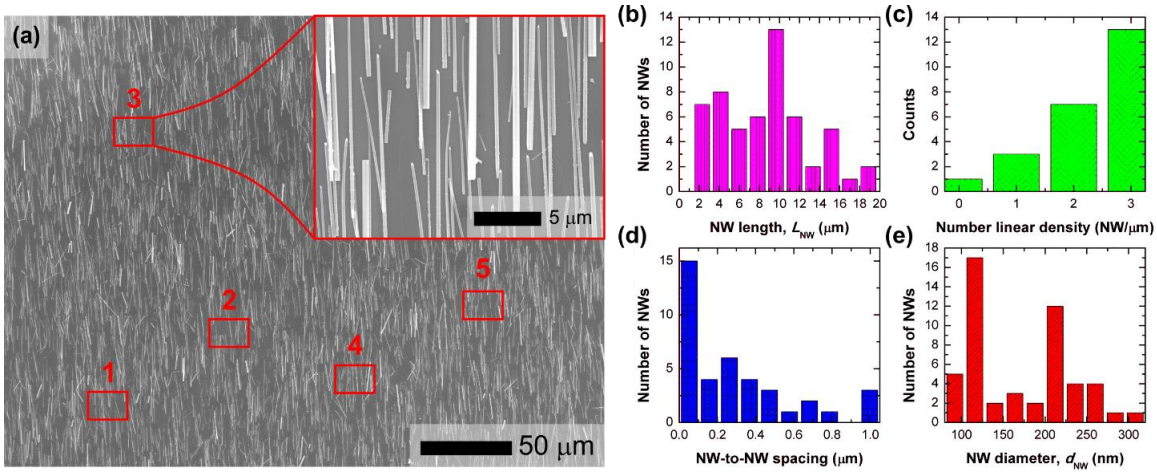


Fig. 7-23: Contact-printing of Si NWs. (a) Optical microscopy and (inset) SEM images of Si contact-printed on Si(100) substrates. Statistical analysis of contact-printing performance carried out on 5 different areas randomly chosen along the total sample area, analysing (b) NW length, (c) NW linear density (d) NW-to-NW spacing, and (e) NW diameter, along a 10-μm long horizontal profile (see inset of (a)). [233]Carried out in collaboration with CGN, FL, DS. Nature: Microsystems & Nanoengineering, 4, 22 (2018) CC BY 2.0.

Contact-printing of both ZnO and Si NWs donor substrates, with dimensions of 1×1 cm^2, has been carried out using the system described in section 3.1.6.1, and under different conditions, comprising contact forces of 1, 2, 3, 4 and 5 N, at a constant $v_{sliding}$ and $l_{sliding}$ of 100 μm/s and 1 mm, respectively. In this section, the analysis of the effect of the contact force, and its equivalent contact pressure, on parameters such as NW linear density and NW-to-NW spacing obtained right after the contact-printing of above NWs on Si(100) substrates is presented. This study aims to determine the optimum conditions allowed by the system for high-performance contact-printing of uniform NWs SAMs over large areas, and analysing any particularity in the printing mechanism of NWs grown by bottom-up and top-down approaches.

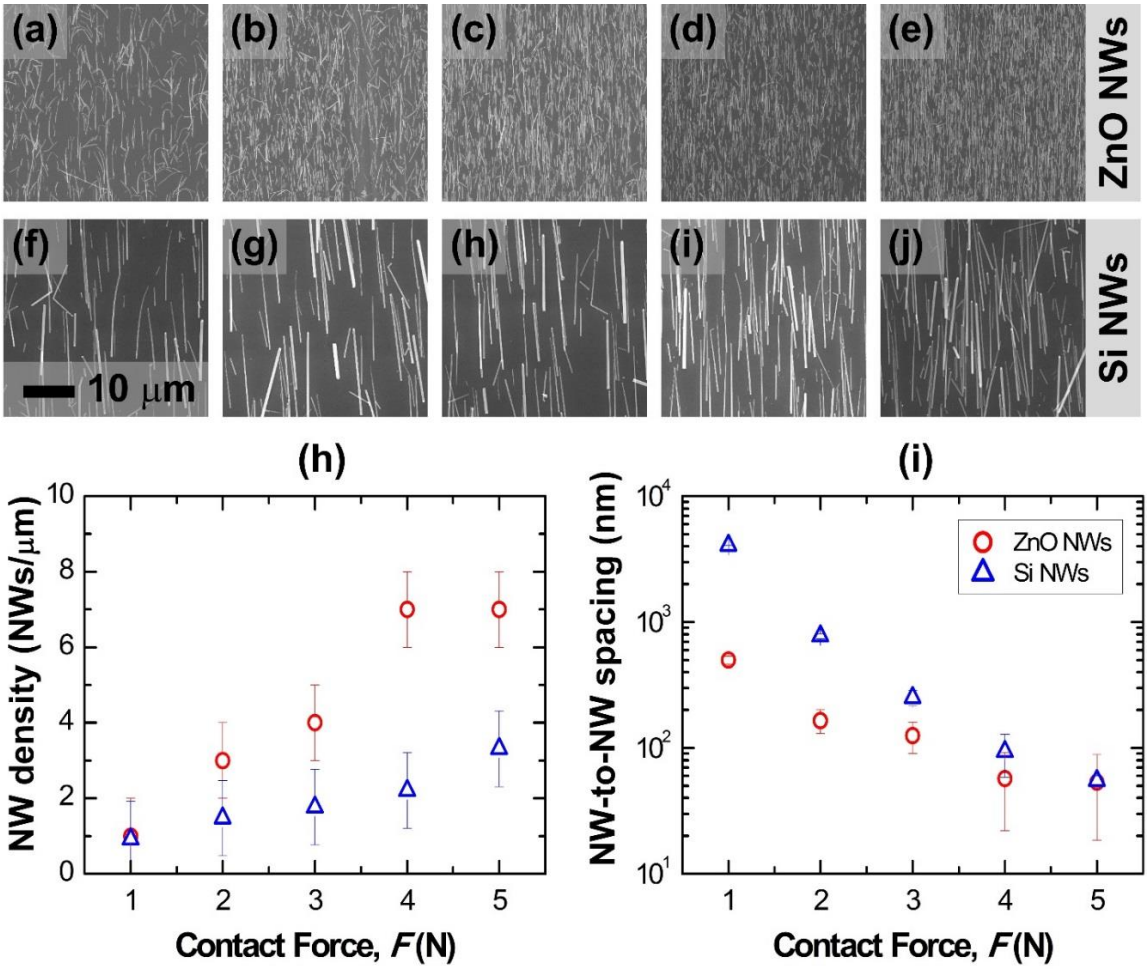


Fig. 7-24: SEM images of (a-e) ZnO and (f-j) Si NWs contact-printed on Si(100) substrates using (a,f) 1N, (b,g) 2N, (c,h) 3N, (d,i) 4N, and (e,j) 5N, and a constant $v_{sliding}$ of 100 μm/s along a $l_{sliding}$ of 1 mm. (k) NW linear density and (l) NW-to-NW spacing obtained from (a-j) and represented as a function of the contact force for ZnO and Si NWs. [233]Carried out in collaboration with CGN, FL, DS. Nature: Microsystems & Nanoengineering, 4, 22 (2018) CC BY 2.0.

Fig. 7-24 shows representative SEM images of contact-printing experiments carried out using ZnO NWs (Fig. 7-24(a-e)) and Si NWs (Fig. 7-24(f-j)) and different contact forces (F) ranged, comprising (a,f) 1N, (b,g) 2N, (c,h) 3N, (d,i) 4N, and (e,j) 5N. From aforementioned SEM images, one can conclude that: i) both kinds of NWs are successfully contact-printed independently on F, for the specific range of forces analysed here; ii) at F > 2 N for ZnO NWs and F > 3 N for Si NWs, transferred NWs are highly aligned along the sliding direction (>90%); iii) NW linear density increases with F, showing highest values of 7 and 3 NW/μm for ZnO NWs and Si NWs, respectively (Fig. 7-24(h)); iv) the NW-to-NW spacing decreases with F, exhibiting minimum values of 50 and 55 nm for ZnO and Si NWs, respectively (Fig. 7-24(i)). Aforementioned NW density is close to those reported in the literature for contact-printed semiconductor NWs, e.g. Ge NWs (8 NWs/μm),[273] Si NWs (9 NWs/μm)[275] and CNTs (10 NWs/μm),[276] and to the best of our knowledge, is the highest reported in the literature for ZnO NWs using contact-printing technique. Moreover, the high NW density has been demonstrated over large areas up to around 1×1 cm^2, showing the potential scalability of the system (see Appendix F of [29]). The successful transfer-printing of both Si and ZnO NWs over large areas is possible due to accurate control of our system, leading to the soft and conformal contact formed between donor and receiver substrates, and

preserving NW length and preventing structural damage during contact-printing process. This unique feature of our system allows us to print electronic SAMs consisting of different kinds of semiconductor NWs on well-controlled regions from few mm^2 to tens of cm^2, which can be potentially used in a wide number of applications depending on the device architecture requirements.

7.3.2. Application: UV Photodetector:

Since JLFET cannot be realised with higher diameter nanowires, a UV photodetector application was implemented based on the synthesised contact printing and using nanowires. While a UV photodetector does not have application on tactile e-skin, it finds application for wearable e-skin patches as a UV dosimeter[31]. The synthesised MACE nanowires were used as resistive structure for this application.

7.3.2.1. Fabrication Steps

Fig. 7-25(a-e) shows a 3D schematic illustration of the step-by-step experimental procedure used in this work to fabricate UV PDs based on WB configuration. A Si(100) substrate with a 300-nm thick layer of SiO_2 on top was used as a receiver substrate. Firstly, four NW assembling areas (2×10 mm^2) were defined in S1818 positive photoresist by photolithography (Fig. 7-25(a)). Prior to the contact-printing process, the receiver substrate was exposed to an O_2 plasma (total pressure 0.3 mbar, 40 sccm of O_2 flux, and 100 Watt) for 1 min using an Oxygen Barrel Asher (PlasmaFab 505), promoting the hydroxylation of the Si surface, i.e. the formation of –OH groups covering the open areas (Fig. 7-25(a)). However, this hydroxylation treatment results in a meta-stable –OH coating, which means, contact-printing experiments need to be carried out right after the plasma treatment in order to ensure the effectiveness of the receiver substrate surface. Then, Si NWs were contact-printed continuously on the receiver substrate with the photoresist, covering three out of four defined areas (Fig. 7-25(b)). Based on the geometry and dimensions of the electrodes, the total area to be covered by Si NWs SAM is around 6×10 mm^2; therefore, the dimensions of the donor substrate, consisting of Si NWs vertically aligned on a Si substrate, are chosen slightly bigger than the electrodes area (7×10 mm^2) reducing the contact-printing stroke. Using the linear positioning stages of the contact-printing system (section 3.1.6.1), the donor substrate is aligned at the specific region where Si NWs are meant to be printed. Then, both donor and receiver substrates are brought in contact under a force of 5 N, which equals to a pressure of around ~70 kPa, followed by the sliding of the donor along a stroke of 1 mm at a speed of 100 μm/s. In the same way, a ZnO NWs based donor substrate with dimensions of around 3×10 mm^2 is contact-printed on the remaining area (2×10 mm^2) using a sliding speed of 100 μm/s and a force of 2.1 N, resulting in the same pressure of around 70 kPa (Fig. 7-25(c)). For the calculation of the pressure, we have assumed that approximately the total area of the donor substrate is in contact with the receiver substrate.

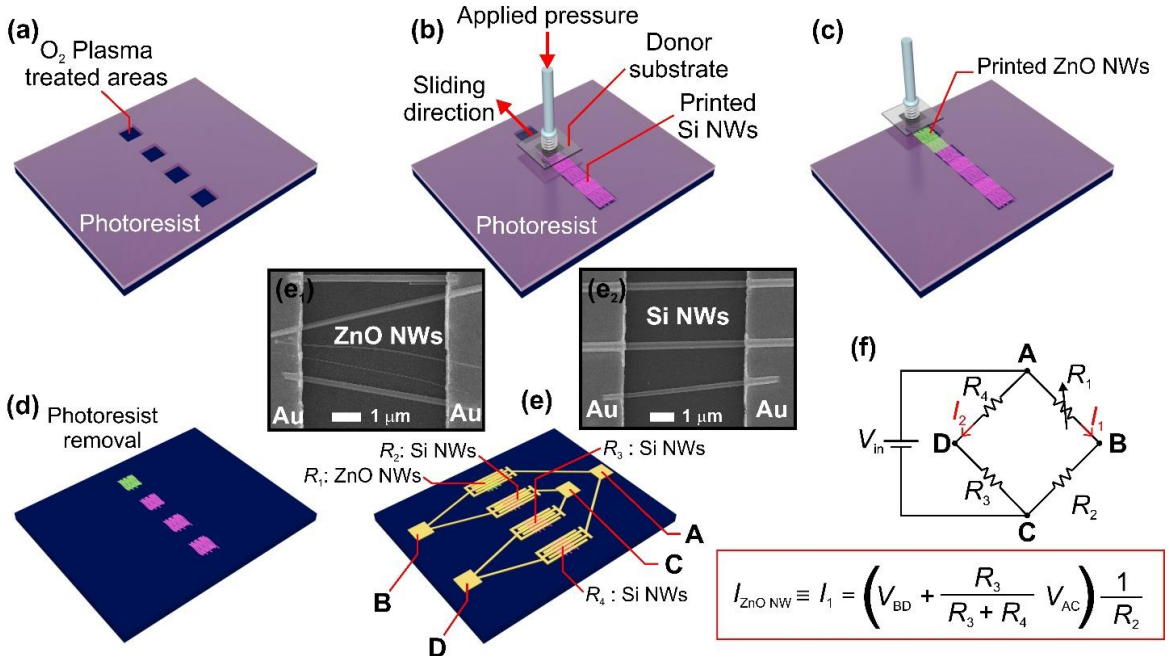


Fig. 7-25: (a-e) Fabrication steps of UV PDs based on ZnO and Si NWs, comprising: (a) definition of 20 mm^2 areas on a S1818 photoresist layer by photolithography, followed by an O_2 plasma treatment (100 Watt and 0.3 mbar for 1 min); contact-printing of (b) Si and (c) ZnO NWs; (d) removal of the photoresist in warm acetone (50 ºC for 2 min); (e) definition of Ti(4nm)/Au(200nm) interdigitated electrodes by photolithography and lift-off, where (e_1) and (e_2) shows SEM images of printed ZnO and Si NWs, respectively, bridging a pair of Ti/Au electrodes with a 5 μm gap. (f) WB equivalent circuit and the expression determining the electric current flowing through ZnO NWs ($I_{ZnO\,NW}$). [233]Carried out in collaboration with CGN, FL, DS. Nature: Microsystems & Nanoengineering, 4, 22 (2018) CC BY 2.0.

After both ZnO and Si NWs are printed on the receiver substrate, sample morphology has been re-analysed by SEM in order to evaluate the success of the contact-printing performance on top of patterned photoresist compared to the process carried out directly on Si(100) substrates (Fig. 7-22 and Fig. 7-23). Results of this analysis show similar assembling performance like those shown in Fig. 7-22 and Fig. 7-23, i.e. NW linear densities around 5-6 and 2-3 NWs/μm for ZnO and Si NWs, respectively. However, after the photoresist is softly removed in warm acetone (50 ºC) for 2 min, and the organic leftovers cleaned in isopropanol (IPA) for 2 min (Fig. 7-25(d)), the average NW linear density of ZnO and Si NWs in the patterned area decreases down to 1 and 0.5 NW/μm, respectively, mainly due to the unintentional removal of NWs during the solvent cleaning. The hydroxylated surface of the receiver substrate has demonstrated to have a strong effect during the contact-printing process but has shown a poor adhesion formed between substrate and aligned NWs during the post-processing of the device. In this regard, wet pre-treatments carried out in receiver substrates and comprising functionalisation processes,[273] have demonstrated to improve the adhesion between NWs and substrate, and therefore, being an excellent alternative to preserve the NW density even under several device post-processing steps, or even allowing a monolithic fabrication.[92]

Finally, four arrays of metallic interdigitated electrodes Ti(4nm)/Au(200nm) with a gap length and width of 5 μm and 10 mm, respectively, and a total number of 12 gaps per array, are deposited by e-beam evaporation technique and defined by photolithography and lift-off

(Fig. 7-25(e)). The linear geometry of the interdigitated electrodes presented in (Fig. 7-25(e)) has been designed in order to favour the integration of NWs using only two steps contact-printing, one for each kind of NW. SEM characterisation carried out after the definition of the electrodes shows that ZnO (Fig. 7-25(e_1)) and Si (Fig. 7-25(e_2)) NW density is almost preserved (i.e. ~1 ZnO NW/μm and ~0.5 Si NW/μm) which demonstrates the robustness and stability of the bridge formed between electrodes. The connections shown in Fig. 7-25(e) are schematically described in the equivalent circuit of Fig. 7-25(f), where ZnO NWs act as R_1, and Si NWs act as R_2, R_3, and R_4 in a WB configuration. R_1 to R_4 have been measured individually (i.e. cutting the device into four pieces and electrically insulating each resistance from others), resulting in R_1 of 571±50 Ω, R_2 of 16±8 Ω, R_3 of 10±3 Ω, R_4 of 11±3 Ω, with the error calculated from the results obtained from 3 different WB devices fabricated by contact-printing. Based on WB expressions (see Appendix G of [29]), the resistances obtained from aforementioned contact-printing process result in an unbalanced WB, i.e. $V_{out} \equiv V_D - V_B \neq 0$. Typically, balanced WB configuration is used in sensing applications mainly due to the high sensitivity of V_{out} to external factors such as light. Following the procedure described in Fig. 7-25(a-e), we have increased R_2 from 16 Ω up to 572 Ω by reducing the contact-printing area of Si NWs from 2×10 mm^2 down to 2×5 mm^2 only in one of the electrodes arrays, whereas contact-printing the other three regions with the original area of 2×10 mm^2. In this scenario, the initial V_{out} measured in dark conditions is around 400 μV, which is considered a balanced WB state ($R_1/R_2 \sim R_4/R_3$, see Appendix G of [29]).

Fig. 7-25(f) also presents the expression of the current flowing through the ZnO NWs resistance ($I_1 = I_{ZnO\ NWs}$) as a function of the WB components, and input (V_{AC}) and output voltages (V_{BD}). This expression was used to calculate the ZnO NWs response under different light environments.

7.3.2.2. UV Photodetector Characterisation

For the sake of comparison, we have characterised the UV photoresponse of both UV PDs based on balanced WB and a single resistance (SR).[277] Firstly, we have characterised up to 3 WB UV PDs using a Probe Station (Fig. *7-26*) and a Semiconductor Device Analyser (Keysight B1500A). The Probe Station is provided with a temperature control, allowing to carry out the electrical characterisation of the PD as a function of the temperature (T) ranging from room-temperature (RT) to 80ºC. After the characterisation of the WB UV PDs, these devices were cut (see α cutting line in Fig. *7-26*(a)), insulating the array of electrodes with ZnO NWs, resulting in UV PDs based on SR. Then, the same characterisation is carried out on UV PDs based on SR. Fig. *7-26*(b) presents dark current (I_{dark}) of WB and SR UV PDs, measured at V_{in} of 0.02 V, as a function of T. From that figure, one can deduce that I_{dark} decreases with T independently of the PD type, which can be explained due to a higher reactivity of oxygen species, leading to an increase of the oxygen absorbed along the ZnO NW surface, and therefore, an increase of the surface trapped charge density.[278] For T > 50ºC, the deviation of I_{dark} with respect RT values (ΔI_{dark}) is more evident in SR UV PDs than in WB, exhibiting high ΔI_{dark} of 65% at T = 80ºC (at T = 80ºC, WB shows ΔI_{dark} ~ 20%). These results highlight one of the benefits of using WB circuits for sensing applications, attenuating external effects such as temperature, and a good demonstrator of the kind of applications possible with the developed contact-printing system to fabricate complex configurations based on NWs sensing and electronic layers.

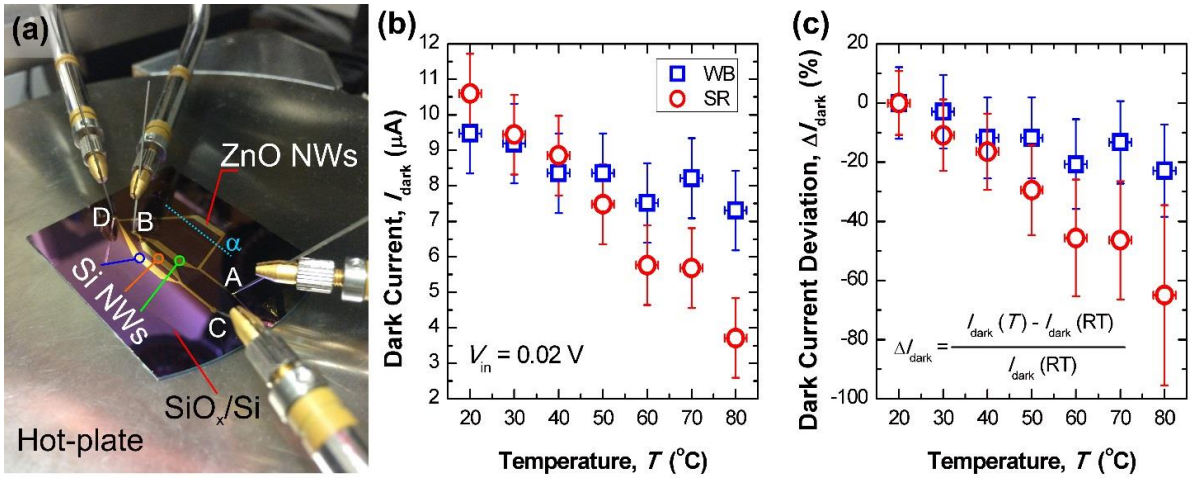


Fig. 7-26: (a) Photographic picture of Wheatstone bridge (WB) UV PD based on contact-printed ZnO and Si NWs; blue dotted line (□) shows the direction and place of the cut carried out to fabricate a UV PD based on a single resistance (SR). (b) Idark and (c) □Idark vs. T for WB and SR UV PDs. [233]Carried out in collaboration with CGN, FL, DS. Nature: Microsystems & Nanoengineering, 4, 22 (2018) CC BY 2.0.

Finally, the photoresponse and response time, including rise time (τ_{rise}) and decay time (τ_{decay}) of UV PDs in WB configuration have been characterised as a function of the UV power density to evaluate the validity of contact-printing to fabricate functional NW based devices. For that, we have used a UV light-emitting diode (LED) ($365 < \lambda < 370$ nm and an optical power of 200 mW at 700 mA) from RS Components (S5050) as UV light source to irradiate NWs based PDs. The power density of this UV LED has been calibrated by using a Si photodiode (BPW21 from Osram) as a function of the LED driving current and distance between the LED and the photodiode (see Appendix H of [29]). For the characterisation presented in Fig. *7-27*, we have positioned the UV LED on top of the PD surface separated by a vertical distance of around 5 cm. Fig. *7-27*(a) presents the dependence of the I_{photo} (measured at V_{in} = 0.05 V) and the power density of the UV source, exposing the PD surface for 5s. From that figure, one can conclude that at lower illumination power densities (< 1 μW/cm^2) the PD exhibits a linear tendency which is consistent with the mechanism governed by the charge carrier photogeneration whose efficiency is proportional to the absorbed photo flux.[278] On the other hand, for higher illumination power densities (> 1 μW/cm^2), I_{photo} changes to a sublinear dependence which can be understood as a lack of hole-traps present at the NW surface, which drastically reduce the photogeneration mechanisms and leading to a saturation of the PD response.

The I_{photo}/I_{dark} ratio has been analysed by exposing the ZnO NWs area of the PD to a UV light with a power density of 4.5 μW/cm^2 and for 30s, while applying to the WB a V_{in} of 0.05 V (Fig. *7-27*(b)). Results demonstrate a high-performance of the fabricated PD, obtaining a I_{photo}/I_{dark} of around 10^4 which confirms the high sensitivity of NW PDs fully fabricated by contact-printing technique. In addition, we have characterised the response time of the UV PDs under single (Fig. *7-27*(b)) and multi-cycles (Fig. *7-27*(c)) of UV illumination. The best fit to data obtained by a double-exponential rise and decay function results in a weight-averaged rise (τ_{rise}) and decay (τ_{decay}) time constants below 1s and around 220s, respectively, which are comparable values to those reported elsewhere for SR based ZnO NWs UV PDs.[277] The durability and reliability of UV PDs characteristics have been evaluated over time and under multi-cyclic UV illuminations, exhibiting a stable

performance (I_{dark}, I_{photo}/I_{dark}, τ_{rise}, τ_{decay}) during cyclic test (Fig. *7-27*(c)) and over several months of characterisation.

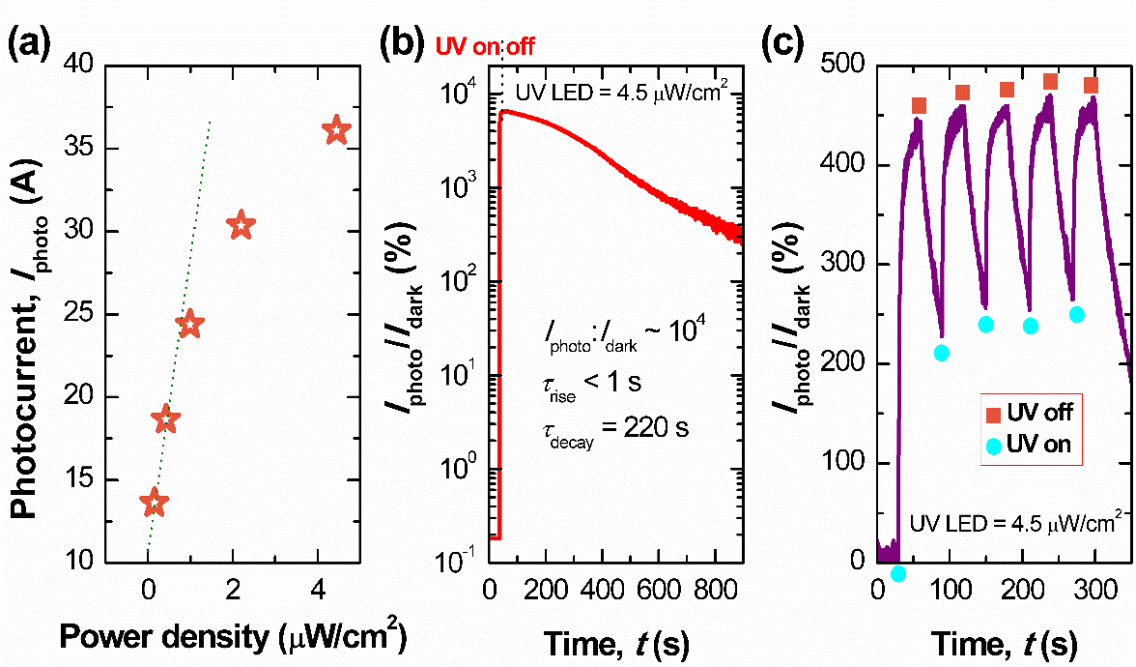


Fig. 7-27: (a) ZnO NW current vs. UV LED power density, measured for 5s under UV illumination, with a distance between NWs and UV LED of 5 cm, and using a V_{in} of 0.05 V. I_{photo}/I_{dark} (b) single cycle and (c) multi-cycles measured over time and using a UV LED power density of 4.5 μW/cm² and a V_{in} of 0.05 V with a 5 cm distance between UV LED and the PD surface. [233]Carried out in collaboration with CGN, FL, DS. Nature: Microsystems & Nanoengineering, 4, 22 (2018) CC BY 2.0.

7.3.3. Large-Area DEP based Transfer Printing of Nanowires to Flexible Substrates

While contact printing is suitable for small aspect ratio or higher diameter nanowires, it is not optimal to use contact printing process to print high aspect ratio nanowires. Further, contact printing is useful for printing wires from wafers. Nanowires synthesised from alternate methods such as solution processed nanowires (refer to section 2.3.3) cannot be printed with the approach presented in the previous section. In this regard, a method for large-area printing of nanowires from suspension is presented in this section. It uses a modified dielectrophoresis (DEP) approach to realize large-area templated assembly of nanowires following which electronics can be realised in the same substrate or the aligned nanowires can be transfer printed to another substrate for realising electronics.

Schematic illustration of conventional DEP is shown in Fig. 7-28. Under inhomogeneous external electric fields, polarizable particles dispersed in liquid media undergo movement. Unlike electrophoresis, dielectrophoresis does not require the particles to be charged. A particle that is more polarizable than its surrounding medium undergoes positive dielectrophoresis, i.e. the particle is attracted towards regions of high field inhomogeneity, while a particle which is less polarizable experiences negative dielectrophoresis, i.e. it is repelled from these regions. The dielectrophoretic force (F_{DEP}) acting on these particles depends on the size, geometry and the dielectric properties of the material and is given by the Claussius-Mosotti equation[279]:

$$F_{DEP} = \frac{\pi r^2 l}{6} \varepsilon_m Re[K_f] \nabla E^2 \quad \textbf{(E7-1)}$$

Where, $Re[K_f]$ is the real part of Claussius-Mossoti (CM) function given by,

$$K_f = \frac{\varepsilon_p{}^* - \varepsilon_m{}^*}{\varepsilon_m{}^*} \quad \textbf{(E7-2)}$$

ε* is the complex permittivity given by,

$$\varepsilon^* = \varepsilon - j\frac{\sigma}{\varepsilon} \quad \textbf{(E7-3)}$$

r, l are the radius and length of the nanowire, respectively, ε_p, ε_m are the permittivities of the particle and the medium respectively, σ_p and σ_m are the conductivities of the particle and the medium, respectively.

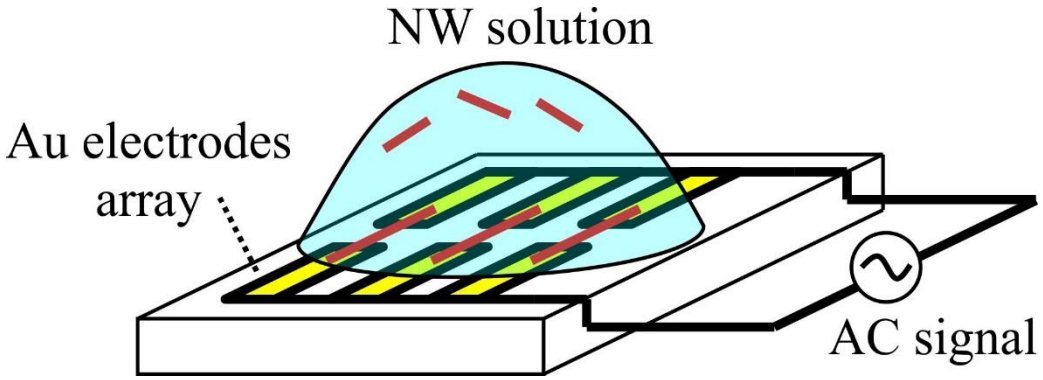


Fig. 7-28: Schematic illustration of conventional DEP

The challenges with conventional DEP for large area are:

1) As the wires bridge, they will electrically load or even short the electrodes thereby affecting or reducing the electric field for further assembly of nanowires.
2) At high field the nanowires which assemble initially may get affected significantly or burnt out because of the heavy current which flows through the wires.

The modified process for large-area DEP assisted printing is schematically shown in Fig. 7-29. Metal electrodes with suitable alignment gaps are fabricated on a rigid or flexible substrate (PI sheets (50 μm) were used for flexible substrate). The inset below shows the cross-sectional illustration at each stage. Then, the electrodes area is covered by a dielectric layer as shown in Fig. 7-29b. This dielectric layer help to solve the above listed two problems with conventional DEP by not letting the nanowires touch the electrodes. Further, once the DEP is over the substrate can be directly used for realising functional electronics with addressable array of cluster of nanowires instead of all the nanowires assembly touching the electrode in conventional DEP. Following the dielectric encapsulation, the sample was dipped in a suspension with nanowires of desired concentration as shown in Fig. 7-29c. An AC signal is applied between the two electrodes. This causes the nanowires to get attracted which eventually assemble over the electrode. The sample is slowly taken out of the suspension. The aligned nanowires could be peeled off from the aligned substrate Fig. 7-29e using a PDMS stamp and transfer to another receiving substrate. With flexible substrate, the same sample with aligned nanowires on specific locations can be directly used for realising devices as the nanowires are on the top of a dielectric and are insulated from the electrodes underneath.

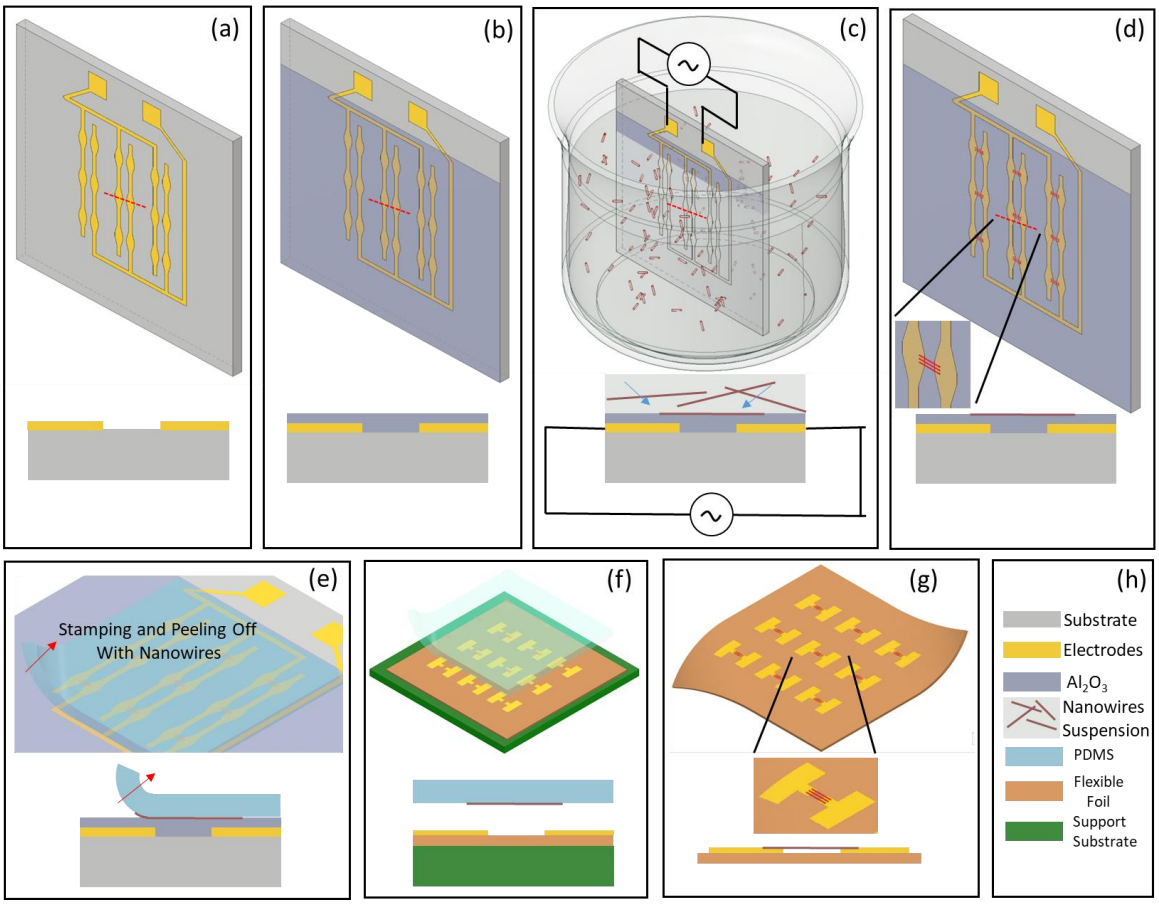
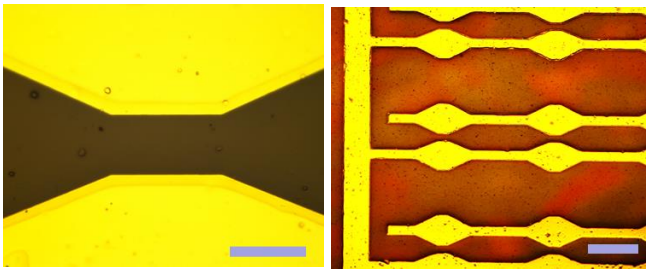


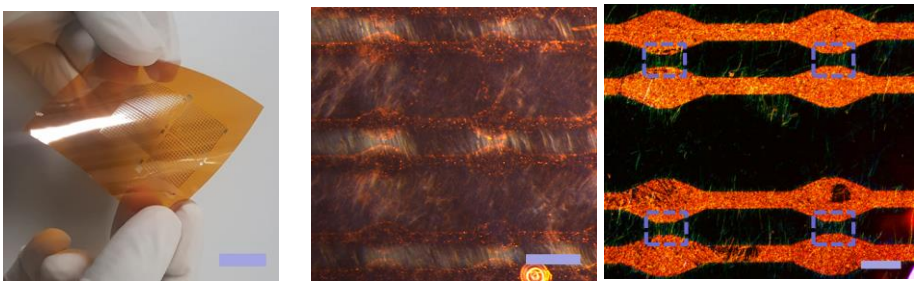
Fig. 7-29: Schematic illustration of large-area DEP

Fig. 7-30 (a&b) shows the microscopic images of the electrodes fabricated on flexible PI substrate (50 µm) for large-area-DEP. The photograph of the fabricated electrode structure is shown in Fig. 7-30c. Fig. 7-30d shows the optical microscopic image of the nanowires during DEP. Due to the challenges associated with synthesis of crystalline sub-30nm nanowires as explained in the previous section, commercial solution-synthesised V_2O_5 nanowires were used to demonstrate the proof of concept. The assembly was to use it for application as non-contact temperature sensor for prosthetic skin taking advantage of the microbolometric phenomenon[280]. A high-density assembly is observed in the area where the electric field is higher.

Fig. 7-31 shows the typical SEM images (3 different magnifications) of assembled nanowires over PVC layer using the above approach. Large-area DEP printing was also used to achieve Printed aligned layers of more than 7 NWs/µm with simultaneous assembly on 30x30 electrodes (minus 4 defect electrodes) patterns in a 3 cm x 3 cm area is achieved through this process. HRTEM imaging of the nanowires were carried out and results are shown in Fig. 7-32. The HRTEM images of single NW provided the lattice fringes corresponding to the NW's crystal structure. This further verified that the individual NWs are single crystalline) and without any notable defects which harm the electronic properties (unlike the Si NWs shown in Fig. 7-21.



a b



c d e

Fig. 7-30: (a&b) Microscopic image of the fabricated electrode structures fabricated on PI for large-area DEP (c) photograph (d) Optical microscopic image of the nanowires assembly during the DEP process (0.1%w/v concentration) on the top of a PVC insulator (e) after DEP (0.02%w/v) (Dashed lines show the assembled regions). (Scalebars: (a)150 µm, (b) 500 µm, (c) 1.5 cm (d) 500 µm (e) 200 µm)

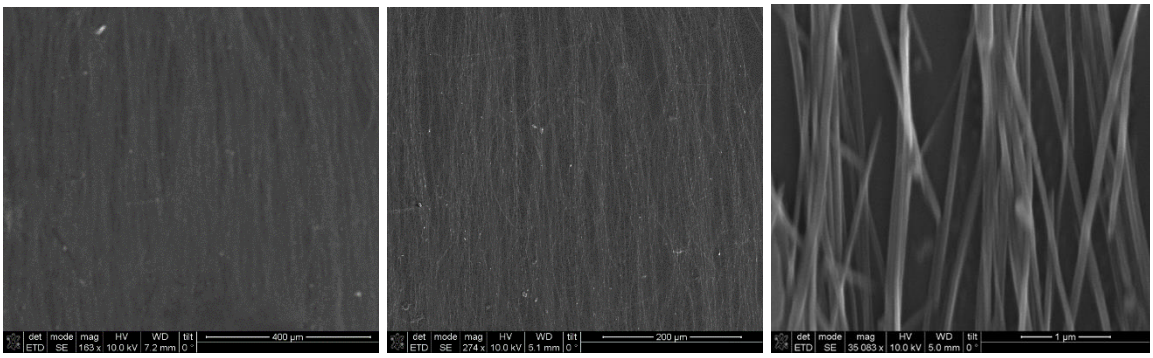


Fig. 7-31: SEM images of large-area DEP-aligned nanowires on flexible PVC substrate

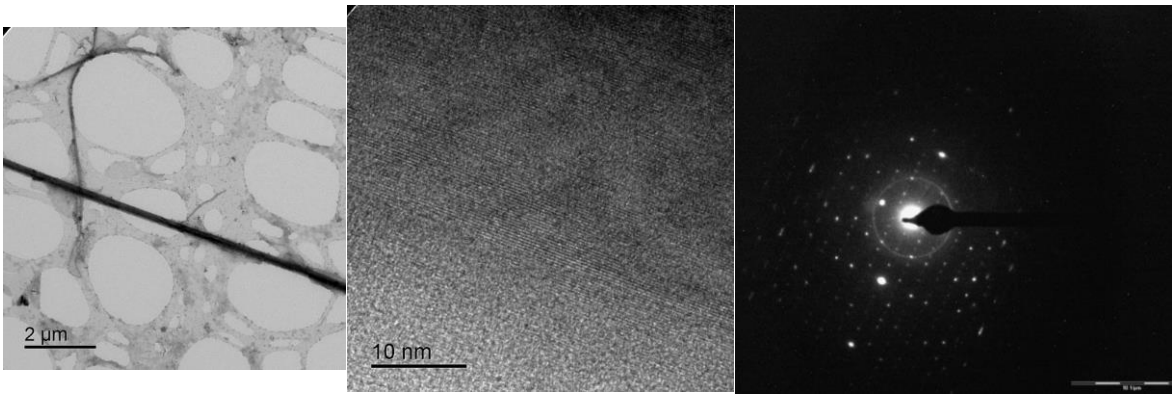


Fig. 7-32: TEM results of the V_2O_5 nanowires

7.3.4. Application: Non-contact Temperature Sensor

Ti\Au (10 nm\100nm) electrode contacts were made with the aligned nanowires and the wires were used as a temperature sensitive bolometric sensor (without focal plane) for non-contact proximal temperature sensing [281] in robotics/prosthesis. The nanowire-based

sensor was tested by attaching it to a water cooled metal plate with a heat source at a distance of 40 cm from it. The temperature of the source was slowly varied, and the resistance of the sensor was measured using a Keysight 6.5-digit precision 34465a multi-meter.

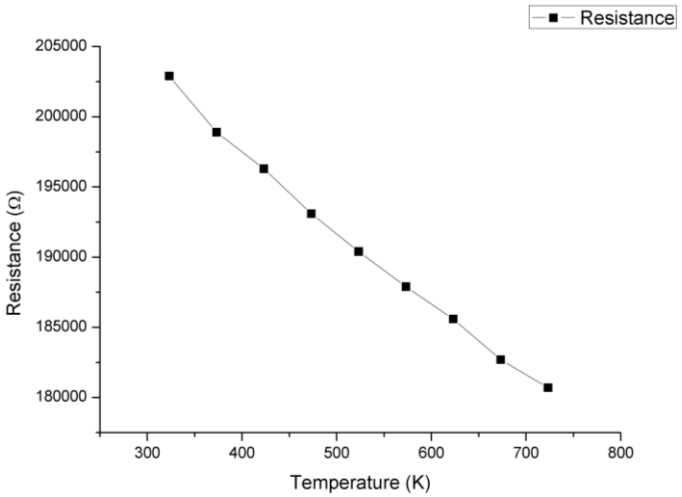


Fig. 7-33: Non-contact temperature vs Resistance characteristics of V_2O_5 Nanowires

Fig. 7-33 shows the non-contact temperatures vs resistance characteristics. The sensitivity was found to be 55.5 Ω/K or 0.03% /K. The measurement is suitable for the tactile e-skin application, however for other high precision applications [281] the sensor concept has to be measured under vacuum and may require focal plane concept with hanging bridge structures.

7. 4. Summary

Overall, Table 20 summarises the results of the experiments of MACE. Nanowires of diameter as low as 10 nm and of aspect ratio more than 200:1 was achieved.

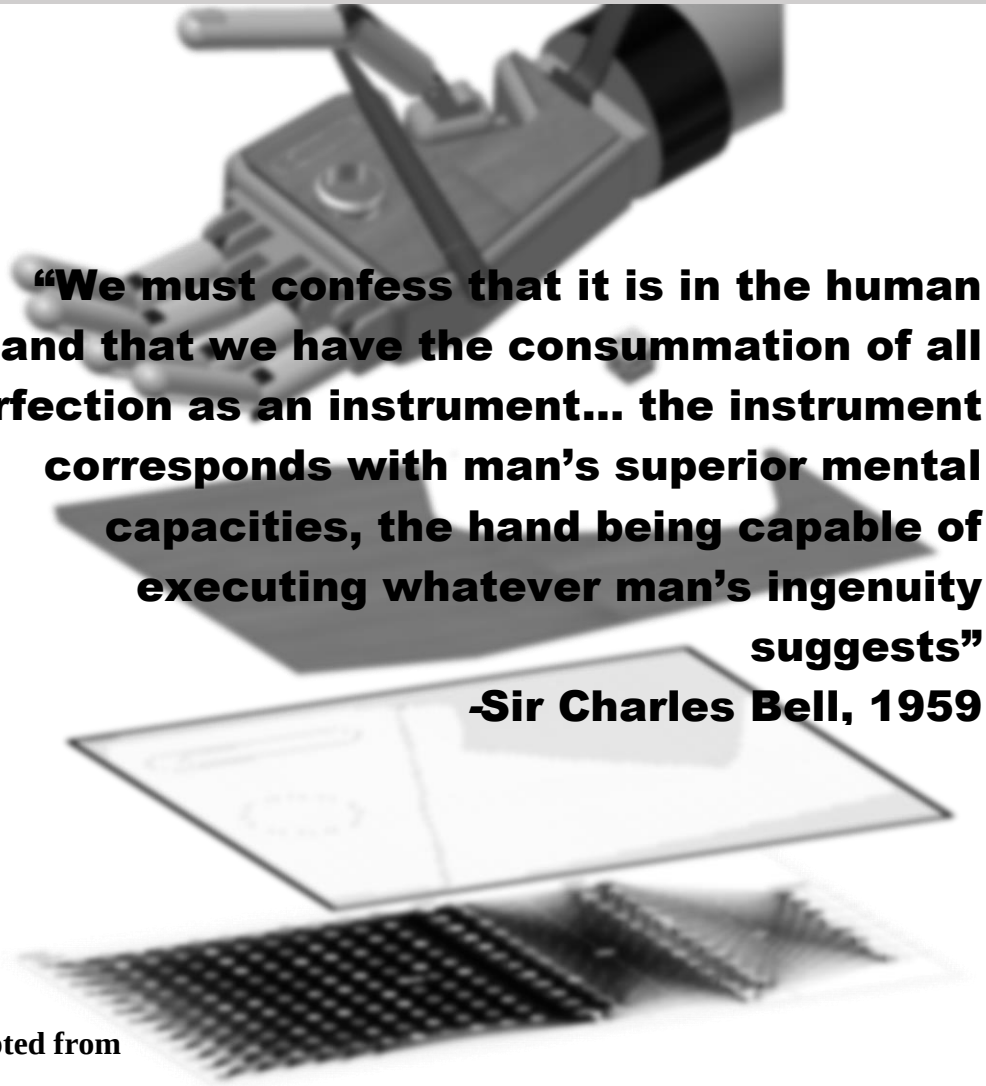
The nanowires of low diameter (sub-30 nm) (for the processing conditions used) resulted in porous nanowires as observed from the TEM images and further optimisation is needed in this regard. Two approaches were used for transfer printing nanowires to flexible substrates. Contact printing was used to realize electronic layers with high NW density (7 NWs/μm for bottom-up ZnO and 3 NWs/μm for top-down Si NWs). The synthesised silicon nanowires were heterogeneously integrated with bottom-up fabricated ZnO nanowires using contact printing to realize ultra-violet (UV) dosimeter structure. The work done on development of large-area DEP-assisted templated transfer printing of nanowires is also presented in this chapter. The process was used to achieve aligned layers of more than 7 NWs/μm (V_2O_5 nanowires) nanowire density with simultaneous assembly on 30x30 electrodes (minus 4 defect electrodes) patterns in a 3 cm x 3 cm area. The assembled wires were used to realize temperature sensors with sensitivity of 55.5 Ω/K or 0.03% /K. The sensor is suitable for tactile e-skin application.

Table 20: Comparison of Various Processes and Typical Parameters Achieved

	Metal Dewetting + MACE	Dots-on-the-fly + MACE	Nanosphere Lithography	Modified NSL
Diameter	Statistically Distributed [~10 nm-200nm]	Controlled by Dose [~25 nm to 100 nm]	Controlled by Sphere Diameter and RIE [~75 nm to 1000 nm]	Controlled by Sphere Diameter [<30 nm]
Pitch/ Spacing	Statistically Distributed [~10 nm-200 nm]	Controlled by Beam Step Size [500 nm]	Controlled by Sphere Diameter and RIE [~100 nm to 1000 nm]	Controlled by Sphere Diameter [~70 nm]
Length	Determined by the etching solution (etch rate) and time of etching Aspect Ratio more than 200:1 has been achieved.			
Porosity	Determined by the etching solution, dimension and time of etching			
Orientation	<100> and <110> achieved. Depends on the crystal orientation of the wafer and the etching solution.			
Cost	Very Low	High	Medium	Medium

8

Neuro-mimicking and Kirigami-inspired e-Skin



“We must confess that it is in the human hand that we have the consummation of all perfection as an instrument… the instrument corresponds with man’s superior mental capacities, the hand being capable of executing whatever man’s ingenuity suggests”
-Sir Charles Bell, 1959

Adapted from

W. T. Navaraj, C. Garcia, D. Sakthivel, V. Vinciguerra, F. Labeau, D. Gregory, and R. Dahiya, "Nanowire FET based Neural Element for Robotic Tactile Sensing Skin," Frontiers in Neuroscience, vol. 11, p. 501, 2017. Frontiers:CC by 4.0.

Contents

8. Neuro-mimicking and Kirigami-inspired e-Skin

As presented in chapter 2 section 2. 4. , the major focus of research on e-skin by various researchers around the world has been on the development of various types of sensors (e.g. contact pressure, temperature, humidity, etc.) and their integration on large-area and flexible/conformable substrates [44,178,46,41,282,283,34,184]. However, as highlighted in section 2.4.3 and Fig. 2-12, processing of a large amount of data from e-skin has remained a challenge, especially in the case of large area e-skin where number of touch sensors increase rapidly. With the recent shift in the focus of tactile skin research in robotics from hands to whole-body tactile feedback, a need has arisen for new techniques to manage the tactile data. Currently, limited solutions are available to deal with large data generated in tactile skin, let alone for the resulting touch-based perception, which is another dimension of tactile data handling. For example, in the case of prosthesis, it is important not only to collect the tactile data for critical feedback, but also to decode the user's intentions in real time [284]. Perhaps a neuron-like inference to handle the tactile data early on could help as indicated by a significant downstream reduction in the numbers of neurons transmitting stimuli in the early sensory pathways in humans [198-200]. Research suggests that distributed computing takes place in the biological tactile sensory system [44,200,177]. For example, the ensemble of tactile data from peripheral neurons is considered to indicate both the contact force and its direction [186,201]. Such distributed local processing of tactile data is advantageous in practical terms as sending reduced data to higher-perceptual level releases some pressure in terms of complex and bulky sensory hardware. Thus, the hardware implemented neuromorphic tactile data processing along with neural networks like algorithms will be helpful. Currently, the neuromorphic hardware is primarily targeted for vision and hearing related applications. Since, vision and hearing are not as distributed as tactile sensing, the neuromorphic hardware developed for them is not optimal for tactile sensing and dedicated solutions are needed. Few works on tactile sensing have used software based neural networks approaches for tasks such as object recognition via texture or materials [285,286]. However, due to the lack of large-scale parallel processing, the software-programmed neural networks are slower and less energy-efficient [287,288] and hence the HNN implementations will be interesting. The hardware neuromorphic architecture implementations reported in literature thus far are based on devices such as memistor [289], spin-logic [290,291], memristor [292], neuron MOSFET [293,294], analog circuit based neurons [295], field programmable gate array (FPGA) [287] and software-programmed neural networks [296]. So far, these technologies have not been used with tactile skin. But, they could offer alternative to the υ-NWFET approach presented here – even if υ-NWFET has many inherent advantages such as possibility of printing devices on large area as discussed in the next section. The above alternative technologies have their own advantages and challenges in terms of complexity, scalability, speed, reliability, repeatability, cost, non-bendability, power consumption etc., which limit their use in the emulation of biological systems. For example, the memistor, a 3-terminal electrochemical cell element achieved limited success because of scalability issues [289]. Likewise, the spintronic neurons are energy efficient [291] but it is challenging to realize practical large-scale neuromorphic architectures and read-out. Recently, two-terminal memristive devices have gained significant attention as the state of their internal resistance could indicate the history of the voltage across and/or current through the device [297]. The memristive approach is promising in terms of low-energy, high-density memories and neuromorphic computing [298], but as memristors are two terminal devices it may not be possible to simultaneously execute the signal transmission (computation or reading phase) and learning

functions (writing phase). Metal NWs finds application mainly as interconnects and junction elements in crossbar memristors. Use of inorganic semiconductor NWs for HNN is an interesting direction.

Addressing the need for tactile HNN in e-skin, this chapter presents a Neural Nanowire Field Effect Transistor (υ-NWFET) structure as the functional building block. The focus of the chapter is on modelling, simulation and first validation with fabricated υ-NWFET structure prior to practical realisation of a large area e-skin. This chapter is organised as follows: The υ-NWFET device structure, working principle related to a biological neuron, and specific advantages of using NWs for HNN are presented in the section 8. 1. Various modelling and simulation tools, and device fabrication methodology are presented in section 8. 1. The results of modelling, simulation and fabrication are presented in section 8.1.2 along with experiment of e-skin integrated on a 3D printed robotic/prosthetic hand. Section 8.1.2.2 discusses overall implementation and study of impact of fabrication related variability over HNN performance. The results are summarised in the concluding section 8. 2.

8. 1. υ-NWFET based neuro-mimicking e-skin

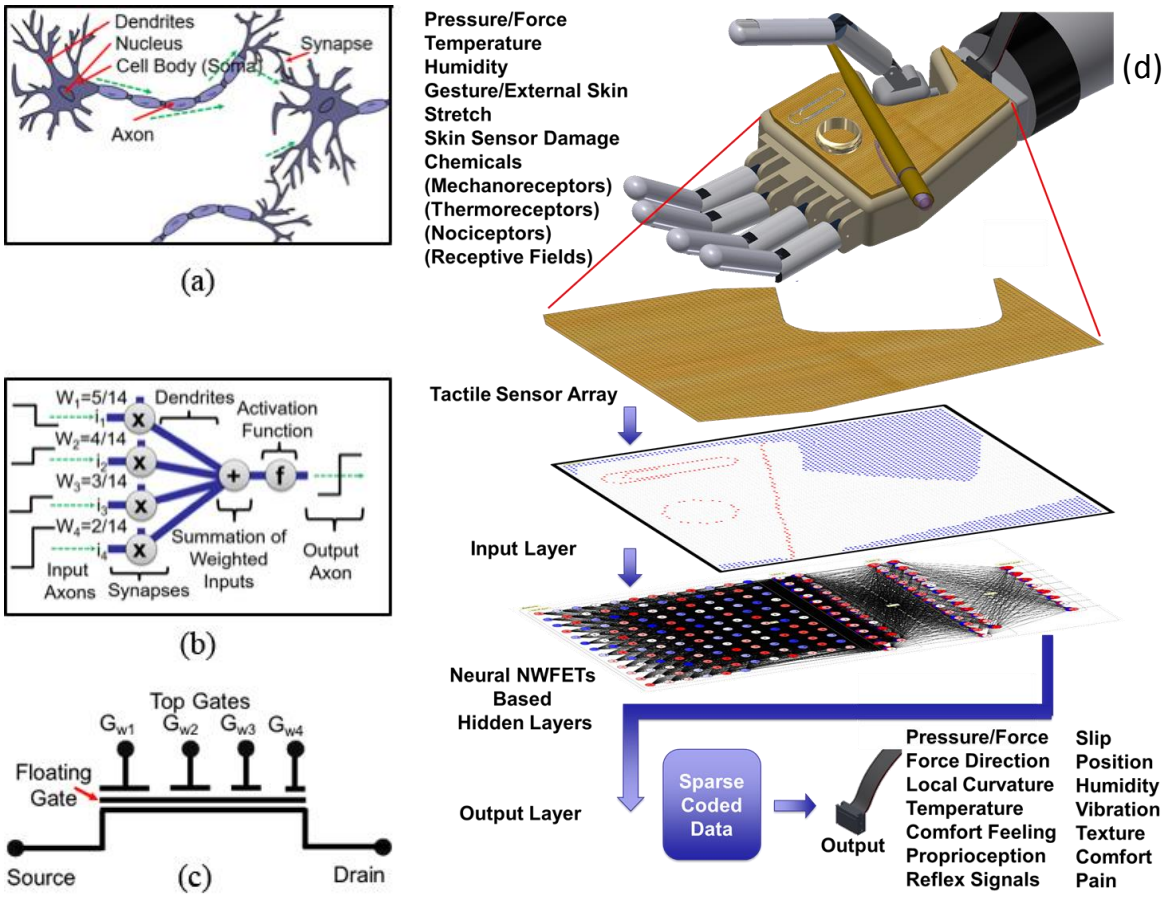


Fig. 8-1: E-skin neural element and proposed tactile data processing scheme: (a) illustration of a biological neuron, (b) block diagram of an artificial neuron corresponding to the implemented weights. Complementary υ-NWFETs followed by an inverter are needed to realize this function, (c) symbolic representation of υ-NWFET, and (d) illustration of ν-NWFET based tactile e-skin covering an artificial hand. The simulated tactile signal is shown as stimuli to the input layer of ν-NWFET based network for coding of tactile information. [33]. Frontiers:CC by 4.0.

A simplified representation of biological and artificial neurons are shown in Fig. 8-1 (a) and Fig. 8-1 (b), respectively [299,24]. The υ-NWFET devices (symbol in Fig. 8-1(c) and structure in Fig. 8-3(a)) imitate the working of biological neuron in a simplified manner. Similar to a biological neuron, the artificial neuron receives one or more inputs. The inputs represent excitatory postsynaptic potentials and inhibitory postsynaptic potentials at neural dendrites. Each input is separately weighted by a weighing factor. The neuron sums them to produce an output activation which represents a neuron's action potential which is transmitted along its axon to the next neuron or other receptors. The structure of υ-NWFET (Fig. 8-3(a)) is a variant of a neuron MOSFET with NWs providing the functional channel region [32,293,300]. The main floating gate, modulating the channel current is capacitively coupled to several gates. The overlap width of the individual gates over the floating gate determines the initial synaptic weight of the neural input on which further schemes of plasticity operates. This imitates the synaptic summation of weighted inputs in the cell body (soma) of the biological neuron or the artificial neuron. The activation function is performed at circuit level as discussed later in Section 8.1.2.1.2. It may be noted that the biological neural systems also have the plasticity or synaptic modulation, which reflects their ability to strengthen or weaken the synaptic weights over time. This modification of weights results in various forms of memory (namely, Sensory Memory, Short Term Memory (STM) and Long Term Memory (LTM) [301,302]) at different hierarchical levels of the neural network. The sensory memory lasts for fraction of a second and is associated with local distributed computation involved in the tactile, smell or vision sensory system. Related to tactile perception, sensory memory plays a role in the local distributed computation such as force direction estimation, local curvature estimation, downstream reductions. Sensory memory on further hierarchical levels leads to STM which typically lasts for few seconds to a maximum of 30 s. These STMs gradually get transformed to LTMs at higher perceptual levels of neural network which can last up to lifetime. The υ-NWFETs based circuits presented here could exhibit similar behavior as discussed later in Section 8.1.2.1.2.

The working of υ-NWFET can be explained with modulation of the source-drain output current by the voltage mode weighted summation of all input voltages to individual gates ($V_{G_{w_i}}$). Voltage-mode summation through an insulating dielectric has significant advantage over current-mode summation as the standby power dissipation can ideally be avoided. The voltage in the floating gate (V_{FG}) is given by:

$$V_{FG} = \frac{\sum_{i=0}^{3} C_{w_i} V_{G_{w_i}}}{C_{FG} + \sum_{i=0}^{3} C_{w_i}} + V_{Offset} \qquad \textbf{(E8-1)}$$

Where C_{w_i} corresponds to the capacitance between the individual gate and the floating gate and determines the weighing factor w_i. $V_{G_{w_i}}$ corresponds to the voltage at each gate, V_{Offset} arises from any non-ideal charges such as fixed-oxide or interface trap charges[262,303].

The schematic illustration of proposed biomimetic tactile sensory neuro-system is given in Fig. 8-1(d). It consists of a prosthetic hand covered with a tactile e-skin; the simulated/measured tactile signal are read out by the receptive sensors to the input sensory layer of the υ-NWFET based neural network for sparse coding of tactile information. In bio-mimicking hardware, the sparse-coded output should comprise of encoded information such as pressure/force and temperature spatial and time distribution, force direction, local curvature, vibration, slip, humidity, comfort feeling, proprioception, reflex signals, pain, gestures. As a demonstration, in this chapter, sparse coding of gesture direction has been presented based on υ-NWFET array architecture. Modelling was carried out to understand

whether NW could be effective as a channel material for a neuron MOSFET as compared to the implementation with bulk material [300]. A combination of p-and n-channel υ-NWFET cascaded with a CMOS inverter has been demonstrated to represent a neuronal element. With multiple synaptic inputs and an output, the proposed structure will contribute towards building a computational architecture inspired by biological systems. An integrated hardware-realised neuromorphic tactile system could mimic or simulate biological activity and lead to unidirectional or bidirectional bio-electronic interfaces.

8.1.1. Methods

The viability of Si-NWs as an active material for HNN has been investigated through modelling and simulation, followed by the fabrication of first υ-NWFET device and tactile e-skin interface. The work flow of methodology used in this chapter is summarised in Fig. 8-2 and described below in detail.

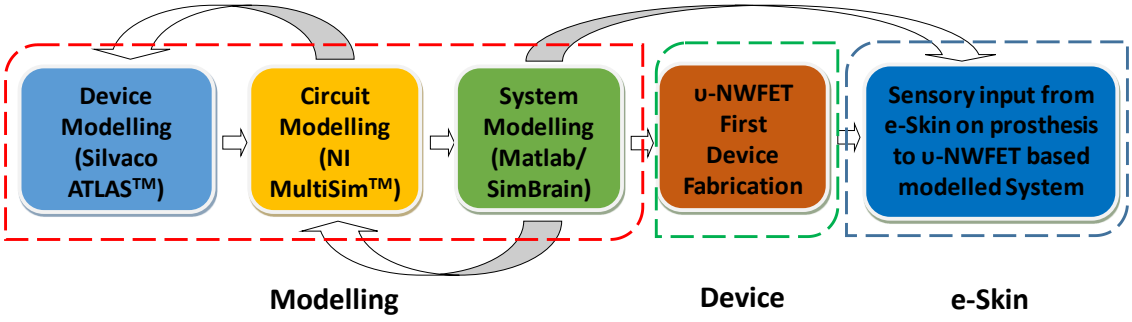


Fig. 8-2: The work flow of the research presented in this section. [33]. Frontiers:CC by 4.0.

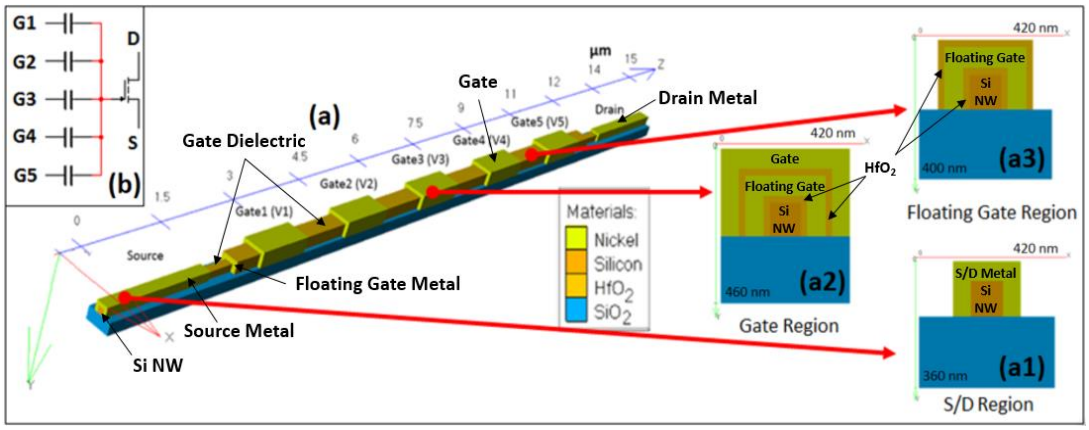


Fig. 8-3: Modelling of ν-NWFET device. (a) 3D Structure of a simulated floating gate ν-NWFET. (a1-a3) Cross-sectional view of the ν-NWFET at drain/source region, floating gate and gate region. (b) Equivalent circuit model of a ν-NWFET. [33]. Frontiers:CC by 4.0.

8.1.1.1. Modelling and Simulation

The structure of proposed υ-NWFET device is shown in Fig. 8-3. The modelling and simulation of the proposed approach was carried out at device, circuit and systems levels as

shown in Fig. 8-2(a). The software tools used for this purpose (also shown in Fig. 8-2(a)) include Silvaco ATLAS™ for device modelling, National Instruments (NI) Multisim™ for circuit modelling and Matlab and SimBrain for training and testing (offline and real-time) of the system model of NN. The implementation of υ-NWFET at device and circuit levels are illustrated in Fig. 8-3(a) and Fig. 8-3(b) (top left inset) respectively. As shown in Fig. 8-3(a), the active channel region of the υ-NWFET consists of a p-type Si-NW with width, height and length (w × h × l) of 100 nm, 100 nm and 15 µm, respectively. The channel region has p-type doping concentration of 10^{14} cm^{-3} and n-type source/drain doping concentration of 10^{20} cm^{-3}. Ni was used for floating gate, top gate and source/drain contacts in this simulation. Of the total 15 µm length of the NW, the channel length corresponds to 10 µm. The simulated υ-NWFET comprises of five gates as input. The cross section of the simulated structure at the drain/source, gate and floating gate area are represented in Fig. 8-3(a1), Fig. 8-3(a2), Fig. 8-3(a3), respectively. A 20.5 nm thick high-K dielectric such as HfO_2 (or Al_2O_3), which corresponds to an effective oxide thickness (EOT) of 4 nm, was used between the input gates and floating gate and between the floating gate and the channel. The gates cover the NWs from three sides forming a tri-gated configuration. The individual gates' span is 1 µm with 1 µm separation gap between them. The υ-NWFET device simulation was carried out in ATLAS-3D to solve the fundamental semiconductor physics equations in three dimension. Further, the concentration dependent and the field dependent mobility models, and Shockley-Read-Hall (SRH) recombination model were defined to be solved by the solver. The default material parameters of Si were used in the solver (details given in Supplementary Section 2 of [33]) while material parameters relevant to the simulation were given as input for user defined materials such as HfO_2 (or Al_2O_3) and Ni. The dielectric permittivity for HfO_2 and work function for Ni used in this work are 20 and 5.01 eV respectively. Fixed oxide charge density of 10^{11} cm^{-2} was defined between semiconductor/dielectric interface. Newton method was used to solve all the equations related to device simulation. All circuit simulations were carried out in Multisim™ with υ-NWFET device model implemented as a modified level-3 BSIM NW MOSFET model. This model is similar to the one used by Lee *et al.* [304], except that the Schottky contact in source and drain were not considered as we have used heavily-doped source/drain junctions in this work. The parameters such as effective oxide thickness of high-K dielectric, electron and hole mobility, effective width and length etc., which were used in the device simulation, were also used in the circuit simulation (Refer to Supplementary Section 2 of of [33]).

8.1.1.2. Fabrication and Characterisation of υ-NWFET Device:

While the printing-strategy presented in previous chapter could be used to fabricate υ-NWFET devices, for a proof-of-concept conventional CMOS fabrication strategy is used to realize a first test device. The fabrication steps carried out for realising the υ-NWFET are shown in Fig. 8-4. The device was realised on a Silicon-On-Insulator (SOI) wafer using standard top-down fabrication steps. The SOI wafer with the active layer thickness of 100 nm over buried oxide (BOX) of thickness 3 µm has been used as a starting material (Fig. 8-4(a)). The supporting bulk Si had a thickness of ~626 µm. The active thin layer is p-type doped with boron has a resistivity of 14-22 Ω-cm. Here, electron beam lithography (EBL) has been used to define the pattern, with a double layer of PMMA2010 4% and PMMA2041 4% as the e-beam resist (Fig. 8-4(b)). After EBL exposure (Fig. 8-4(c)) and development, NiCr metal film of thickness 50 nm was deposited using an electron beam evaporation technique (Fig. 8-4(d)), followed by a standard lift off process (Fig. 8-4(e)).

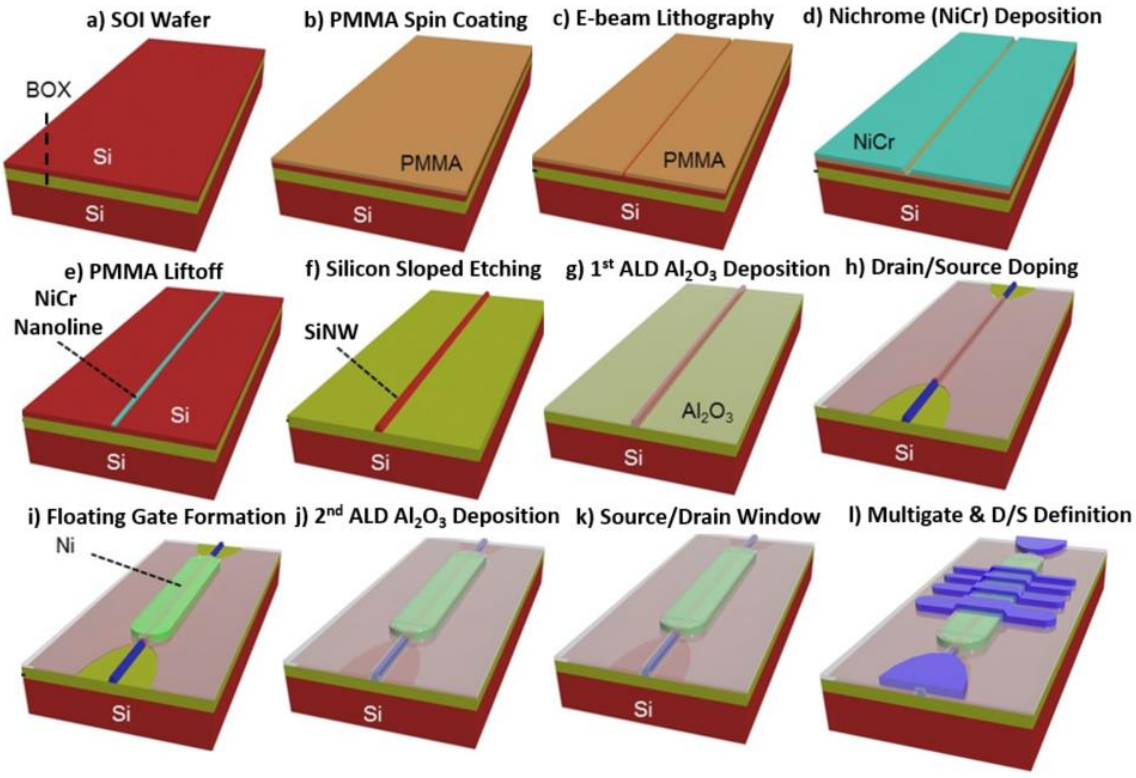


Fig. 8-4: Schematic illustration of fabrication steps for ʊ-NWFET. [33]. Frontiers:CC by 4.0.

The resulting NiCr nanoline (200 nm wide) acted as the hard mask during dry etching to get Si NWs. During dry etching process, a mixture of semiconductor grade $SiCl_4$ and Ar gas was introduced in Reactive Ion Etching (RIE) system. The etching process used an optimised recipe to obtain a tilted slope of etch with nearly 45º angle. A mixture of 7.5 sccm $SiCl_4$ and 15 sccm Ar was introduced in the etching process. This resulted in a trapezoidal shape which led to conformable coverage during subsequent processes. The hard mask was then removed by using NiCr etchant. A high-k dielectric layer (Al_2O_3) of thickness 50 nm was deposited conformably over the Si-NWs (Fig. 8-4(g)) using atomic layer deposition (ALD) to insulate the forth-deposited Ni floating gate later in step shown in Fig. 8-4(i). This was followed by source drain doping and actuation. The source and drain were doped into targeted p+ doping concentration of ~$10^{20}/cm^3$. Since the starting substrate is p-type the above step resulted in a depletion mode ʊ-NWFET. Although this contrasts with the enhancement mode FET explained in the simulation section, it still serves the purpose when it comes to demonstrating the working of the ʊ-NWFET. The morphology of Si-NW was characterised by using AFM before and after Al_2O_3 deposition (Fig. 8-4(g)) and doping (Fig. 8-4(h)). Thereafter, a 30-nm thick Ni film was deposited over S1818 photoresist on an Al_2O_3 layer. This was followed by lift-off to obtain a floating gate for the neural FET (Fig. 8-4(i)). The floating gate was encapsulated with another 30-nm thick Al_2O_3 layer deposited on top by ALD (Fig. 8-4(j)). This was followed by the definition of source, drain and multi gate electrodes with 100nm/10 nm Pt/Ti evaporated over UV lithography patterned photoresist and lift off (Fig. 8-4(k & l)). Finally, the devices were sintered in forming gas (5% H_2 + 95% N_2) at 400ºC for 20 minutes to conclude the the device fabrication process. Since the capacitance plays a crucial role in

the υ-NWFET, the Pt/Ti-Al_2O_3 (80 nm)-Si stack was studied using Capacitance-Voltage (C-V) characterisation with a Keysight 1520A capacitance measure unit. The Current-Voltage (I-V) characteristics of υ-NWFET was also measured using Keysight 1500A semiconductor parameter analyzer. Analysis of the I-V characteristics indicates some device induced variation in gate weights, which could potentially lead to variations in the performance of the HNN.

8.1.1.3. Fabrication of Tactile Sensitive Kirigami-inspired E-Skin

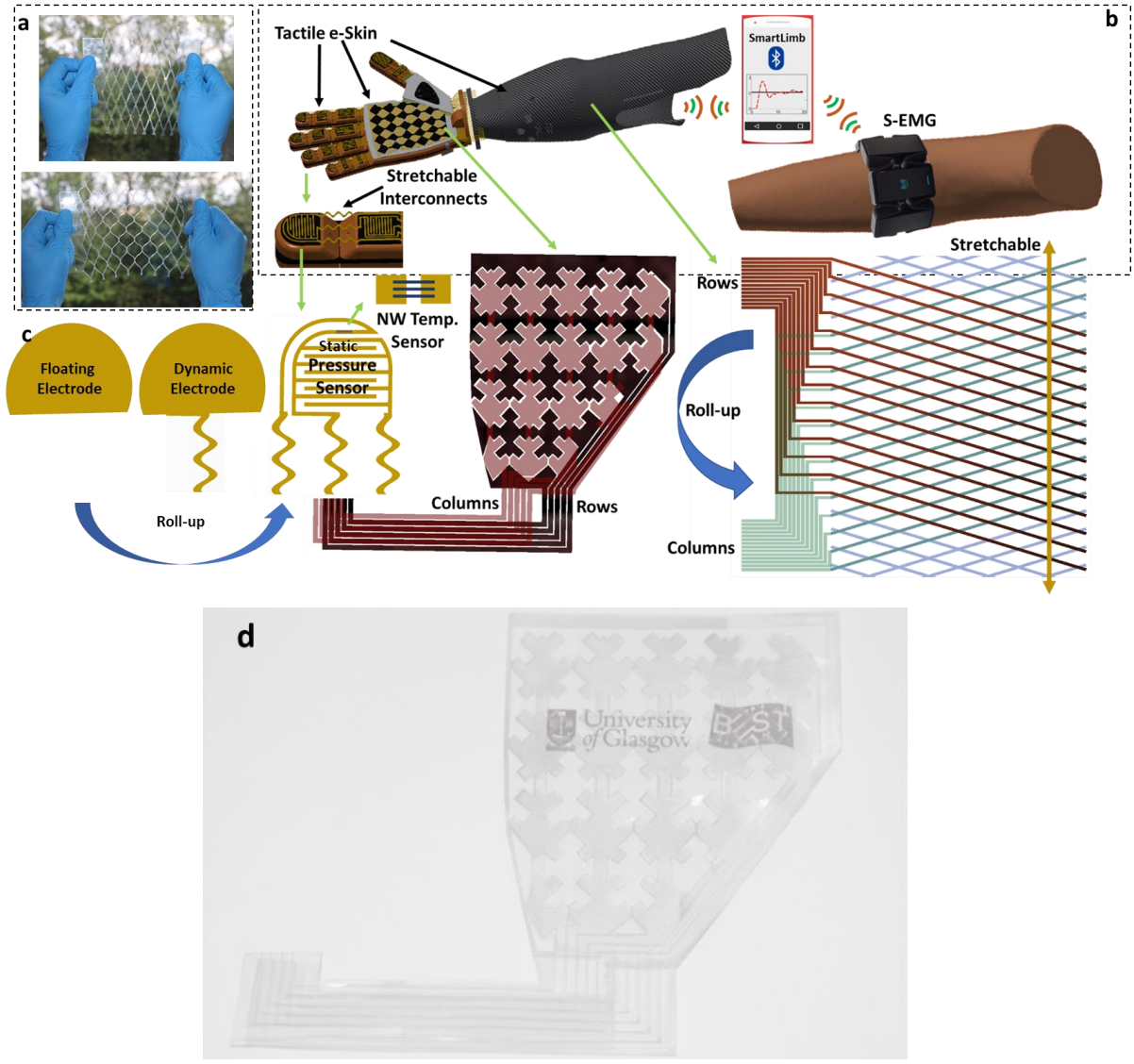


Fig. 8-5: Kirigami-inspired skin for prosthetic hand. [33]. Frontiers:CC by 4.0.

To test the various concepts (passive and active sensors with IMNS) a myo-electric controlled 3D printed prosthetic/robotic hand was designed (in Autodesk Inventor), fabricated (by 3D printing) and tested for mechanical functionality. This serves as a test platform for further research. To form a conformal sensory array structure on the prosthetic hand, a kirigami-inspired skin was envisaged. The various components of the skin are shown in Fig. 8-5. The skin is realised expanding upon the concept discussed in chapter 4 again by laser patterning of ITO sheet. However, because of the size requirement to cover the skin commercial ITO sheet from Sigma Aldrich was used for this work (comprising of ITO film of thickness 130 nm and sheet resistance of 60 Ω/□ over PET of thickness 200 μm). Fig. 8-5a shows kirigami cut ITO structure before and after stretching. The Kirigami skin is

divided into three modules (i) Fingers, (ii) Palm region, (iii) Forearm. The sensor structure for one of the phalanges of the skin are shown in Fig. 8-5c which are fabricated in a cut and rollup approach of the structure discussed in section 4. 2. The 6x6 touch sensor array on the palm has interlaced diamond patterns of ITO over an area of ~3x3 in^2. The skin on the forearm was realised in a one-sided stretchable form with a cuff structure on the other side comprising row-column electrodes.

The palm area of the skin was used to demonstrate the real-time working of proposed approach ν-NWFET approach. This is a step towards our future goal of obtaining a large scale υ-NWFET based printable electronic skin. The sensor array in the palm area of the skin was interfaced with the SimBrain model through a capacitive array readout circuitry. The capacitive touch sensor array and the readout circuit was similar to our recently reported work [34]. However, in the present case we have used laser-ablation based patterning of indium tin oxide (ITO) on polyethylene terephthalate (PET) substrate instead of blade-cutting based patterning of Graphene on Poly-Vinyl Chloride (PVC) substrate. Finally, the tactile sensitive e-skin was interfaced to SimBrain model and was tested in real time. To achieve this, the source code of SimBrain was modified to include a capacitive e-skin readout module programmed in Java. This final model was also used to understand the potential impact on neural function of the resulting network due to the deviation in gate weights arising from the line-edge roughness during fabrication, as described in previous subsection.

8.1.2. Results

8.1.2.1. Modelling Results

8.1.2.1.1. Device Modelling

The weighted sum of voltages in the input gates determines the current I_{DS} between the drain and source.

Fig. 8-6(a) and

Fig. 8-6(b) show the transfer and output characteristics of υ-NWFET respectively as the gates are turned-on one by one. In

Fig. 8-6(a), the V_{GS} sweeps were carried out with common mode V_{GS} applied to a single gate and then progressively up to five gates. Working in the enhancement mode, the υ-NWFET is normally off. As the common-mode voltage is applied to two or more gates, the effective voltage in the floating gate of the transistor (Eq (1)) increases and results in an increased current flow I_{DS} through the transistor.

Fig. 8-6(b), shows V_{DS} Vs I_{DS} characteristics as 5V is applied progressively from one gate to five gates.

8.1.2.1.2. Circuit Modelling

The equivalent circuit of a υ-NWFET was also implemented in NI MultiSim with equal weights by connecting capacitances (corresponding to the dimensions of a υ-NWFET used in the device simulation) to an n-MOSFET (Fig. 8-3(b)). To realize the logistic output typical of an artificial neuron, a complementary υ-NWFET-based inverter and complementary NWFET-based inverter were connected in series, as shown in Fig. 8-7(a) to provide the activation function. All weights were kept equal, with a capacitance of 0.052 pF corresponding to a gate span of 10 μm. Rest of the parameters were unchanged from the simulated device in Fig. 8-7. The output of this circuit (Fig. 8-7(a)), shown in Fig. 8-7(c),

shows that as the common mode input passes through more gates the neuron turns on at lower voltages. This indicates that the proposed υ-NWFET based neuron can provide a logistic output and could be used directly to realize neural network circuits – with the area of the capacitor's overlap with the channel determining the synaptic weight of the input. Fig. 8-7(b) further highlights this with a circuit such as the one in Fig. 8-7(a), except that the non-equal gate weighted υ-NWFET neuron has been implemented. The common mode input is passed through synaptic weights (1.5, 1.5), (0.5, 1.0, 0.5, 1.0), (0.5, 1.0, 1.5), considering 3 as the maximum weight. The weights were realised with 3 capacitor values (0.026 pF, 0.052 pF and 0.078 pF) at each of the n-type and p-type υ-NWFETs. Fig. 8-7(d) shows that for all these cases (where weight is ~3), the neuron turns on at the same voltage of ~3.12 V.

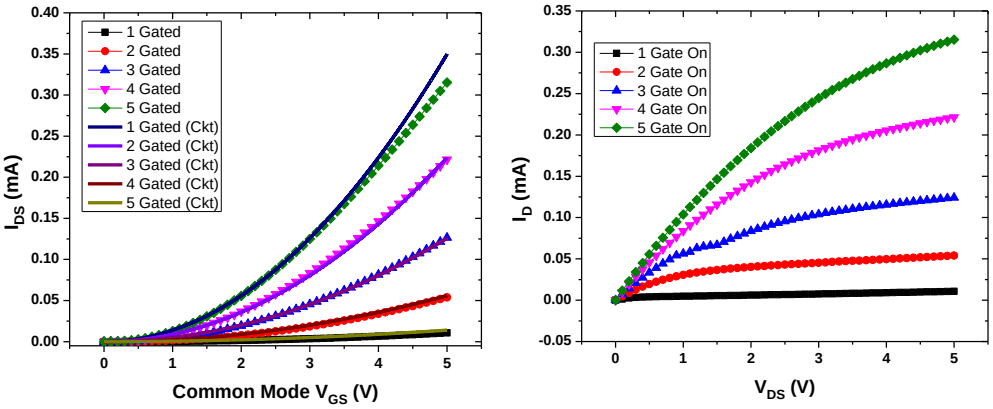


Fig. 8-6: (a) Transfer characteristics from simulation of ν-NWFET device (dotted) and circuit (continuous) based on them. (b) drain current (I_D) vs D-S voltage (V_{DS}) as the gates are turned on one by one. [33]. Frontiers:CC by 4.0.

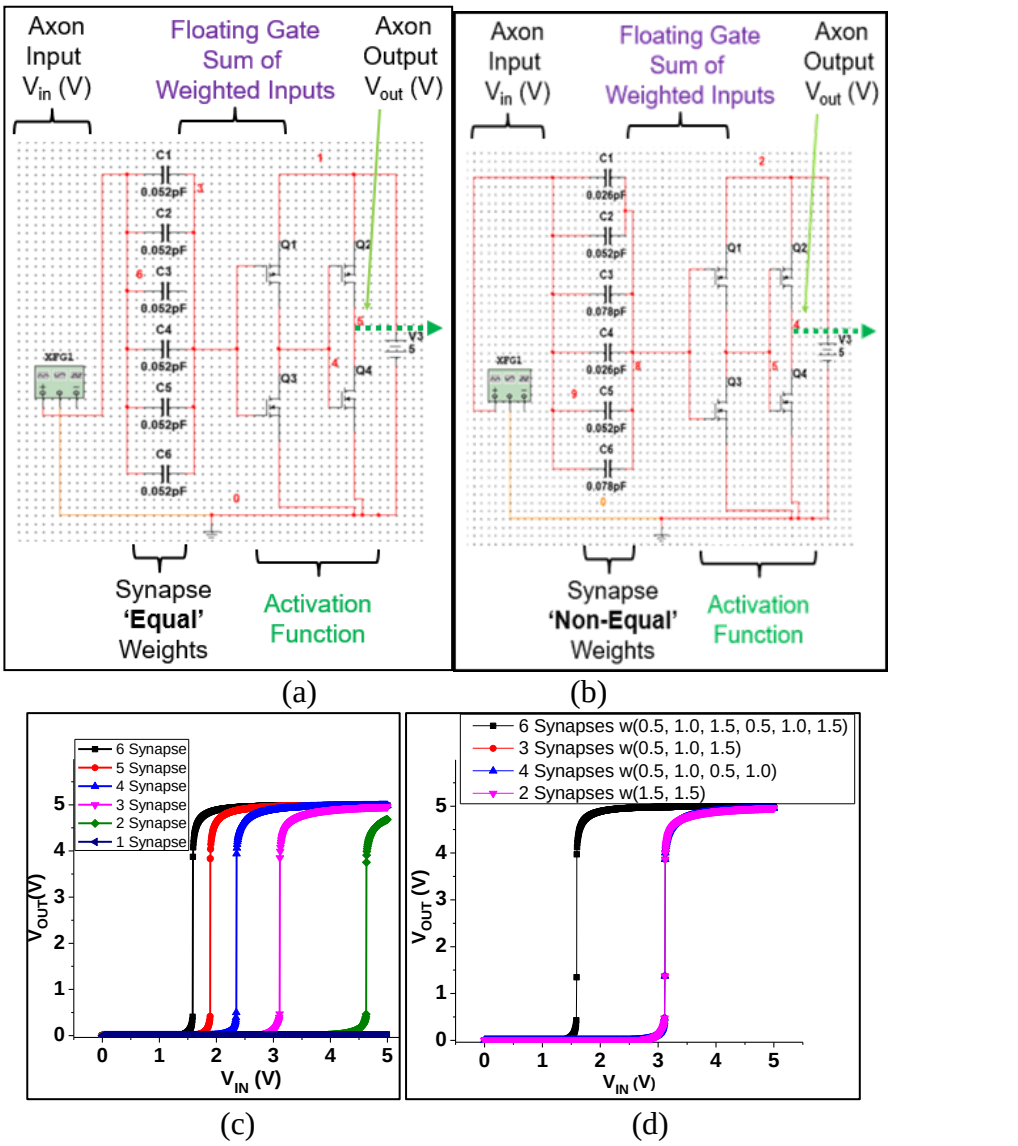
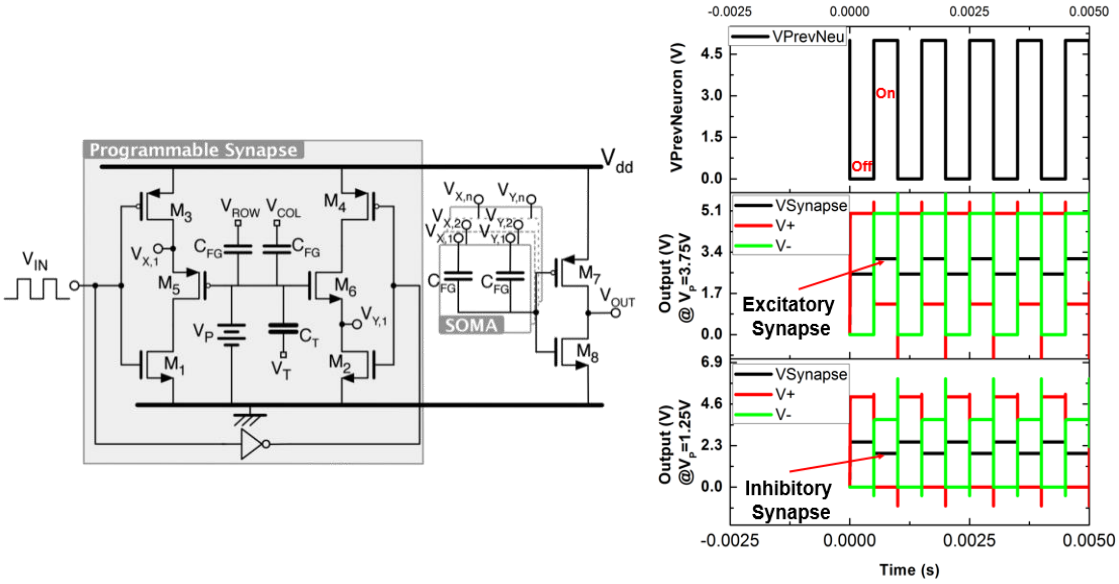


Fig. 8-7: Equivalent circuit implementation of (a) equally and (b) non-equally weighted υ-NWFET based neurons and (c, d) their respective input-output characteristics. [33]. Frontiers:CC by 4.0.

Also Fig. 8-7(d) shows that the doubling of the total weight to ~6, results in the neuron turning on at ~1.59 V. Thus, a neural network implemented with a complementary υ-NWFET based inverter will have the weights hard-wired by the area of the gate span over the channel.



(a) (b)

Fig. 8-8: (a) Schematic and (b) output of a floating gate programmable synapse simulation. [33]. Frontiers:CC by 4.0.

For neuromorphic computing, plasticity or ability to modify the weights of the neurons is also needed. In this regard, the next two circuit level simulations (Fig. 8-8 and Fig. 8-9) are relevant as they indicate the steps towards synapses with plasticity using υ-NWFET approach. In both these cases, υ-NWFET based neurons act as a soma of the neuron while schema proposed for synapses are different. First approach (Fig. 8-8) presents simulation of an EEPROM-like programmable υ-NWFET synapse to emulate the long term biological memory [93,300]. The second approach (Fig. 8-9) shows simulations that are designed to emulate a sensory memory synapse utilising passive components such as NW based resistors and capacitive structures along with υ-NWFET. Further directions have been proposed for this approach to extend it towards STM and LTM exploiting recent work on nanoionics transistors or memristors [305].

The schematic and the outputs of simulation of a neuron with a programmable synapse are shown in Fig. 8-8(a) and Fig. 8-8(b) with complementary υ-NWFET and inverter to form a soma. The EEPROM-like programmable υ-NWFET forms an element of the synapse. Programming is carried out by selecting the V_{ROW} and V_{COL} and then applying the tunnelling voltage V_T to let electrons tunnel through the tunnel capacitor C_T and program the floating gate voltage V_P. This programmed voltage V_P determines the synapse weight and modulates the output $V_{Synapse}$ (= ($V_{X,1}$ + $V_{Y,1}$)/2). It can be observed from Fig. 8-8**(b)** that the gated p-MOS (left) and n-MOS (right) source followers are off whenever the output from the previous layer neuron (V_{IN}) is off. This results in $V_{X,1}$ (V+) = 5 V (i.e. V_{DD}), $V_{Y,1}$ (V-)=0 V (i.e. V_{SS}) and $V_{Synapse}$ = 2.5 V (V_{DD}/2), as shown in the output in Fig. 8-8(b). When the output from the previous layer neuron (V_{IN}) is on, the $V_{Synapse}$ results in an excitatory response for V_P > 2.5 V and an inhibitory response for V_P < 2.5 V. The graph in Fig. 8-8(b) shows the result for V_P of values of 3.75 V and 1.25 V corresponding to excitatory modulation and inhibitory modulation, respectively. This validates the υ-NWFET based circuit through simulation based on NI MultiSim. These neurons could be connected in various configurations to realize systems. However, one drawback of the above approach is that it requires 2 complementary υ-NWFETs per neuron, 2 complementary tunnel υ-NWFET and

4 NWFET per synapse. The EEPROM programming results in a non-volatile long term storage or long term memory. Further a high field is needed across SiO_2 to achieve the tunnelling, which could result in some reliability issues.

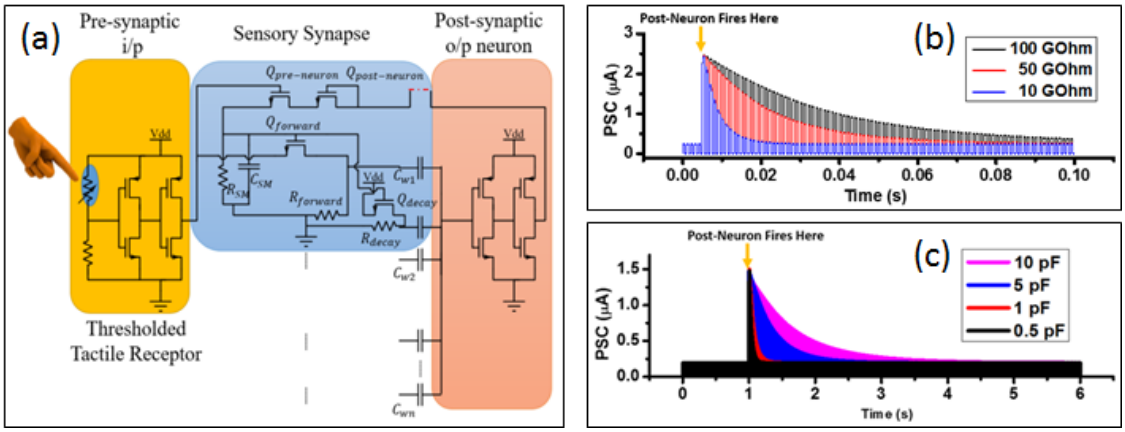


Fig. 8-9: (a) Schematic of a neuron with sensory memory and adaptable towards STM and LTM. (b) Post synaptic current vs. time graph demonstrating sensory memory. (c) Post synaptic current vs. time graph demonstrating short term memory (STM). [33]. Frontiers:CC by 4.0.

For tactile data processing, neurons with sensory memory like biological skin are preferred. In Fig. 8-9(a), we propose a circuit that takes advantage of NW processing to achieve neurons with sensory memory. The features include processing strategies to obtain a controlled array of NWs [129,306,307], the effectiveness of an array architecture [308] and the inherent length of NWs. By taking advantage of the high aspect ratio of NWs, suitable resistance (R_{SM}) and the capacitance (C_{SM}) values can be obtained to realize a pattern designable RC delay operating in non-switched or switched mode. This could be further used to realize both sensory memory and short term memory. For example, a Si-NW with 100 Ω-cm resistivity, 100 μm length and square cross section with a width of 50 nm will have resistance ~40 GΩ. A monolithically integrated 20.5 nm thick HfO_2-based dielectric between two 100 μm long and 500 nm wide metal NWs will give a capacitance of ~1.7 pF. Together these two components will lead to a RC delay of ~69 ms, which is of the order of a typical sensory memory [301]. Fig. 8-9(a) shows the scheme of this approach with a sensory synapse implemented with a thresholder tactile sensory receptor (considered as a presynaptic input). The output of the presynaptic neuron passes through the voltage divider formed by the internal channel resistance of NWFET $Q_{forward}$ and NW resistor $R_{forward}$. This, along with the capacitance C_{w1}, decides the synaptic weight. $C_{w1}-C_{wn}$ might have equal values acting just as a summing unit (soma) as in Fig. 8-7(a) or non-equal value as in Fig. 8-7b. To avoid bootstrapping effect, it is best to have a depletion mode NWFET for $Q_{forward}$. As per Hebbian learning, the correlation between firing of pre- and post-neuron strengthens the synaptic weight between these two neurons. This is achieved by the feedback path, from the output of post-neuron through $Q_{post-neuron}$ and $Q_{pre-neuron}$ to sensory memory element C_{SM}. When the pre- and the post-neuron fire together, the latter charges the C_{SM} and causes the $Q_{forward}$ NWFET's internal resistance to decrease. This eventually increases the synaptic weight between the pre- and post-neuron. Fig. 8-9(b) shows a typical output when the sensory memory NW resistor's (R_{SM}) value is changed between 100, 50 and 10 GΩ, for a pulsed pre-synaptic firing of a neuron with a duration of 500 µs. As soon as the post neuron fires (500 µs) along with pre-neuron, the C_{SM} gets charged. The excitatory

post synaptic current decays exponentially as the C_{SM} discharges through R_{SM}. The neuron will continue to get pre-synaptic input through the voltage divider between Q_{decay} and R_{decay}. The actual effective capacitance contributing to the sensory memory is a combination of gate capacitance of $Q_{forward}$ as well as C_{SM}. Depending on the timing requirement of the sensory memory, C_{SM} could even be avoided, thus making use of the internal capacitance of $Q_{forward}$. The output of the neuron (V_{v-out}) is a function of V_{FG}, which depends on the gate inputs (V_{Gn}) incident on the various capacitors as given by Eq. 1. V_{Gn} is given by the internal resistance $R_{Q-forward}$ of $Q_{Forward}$ and the resistance $R_{Forward}$:

$$V_{Gn}(\mathrm{t}) = V_{v-in}\frac{R_{Q-forward}(V_{MEM}(t))}{R_{Forward}}(1 - e^{-\frac{t}{\tau 1}}) \quad \textbf{(E8-2)}$$

$R_{Q-forward}$ depends on $V_{MEM}(t)$ across C_{SM} which is given by:

$$V_{MEM}(\mathrm{t}) = V_{v-in}\frac{R_{SM}}{R_{TotReverse}}\left(1 - e^{-\frac{t}{\tau 2}}\right) \quad \textbf{(E8-3)}$$

Where,

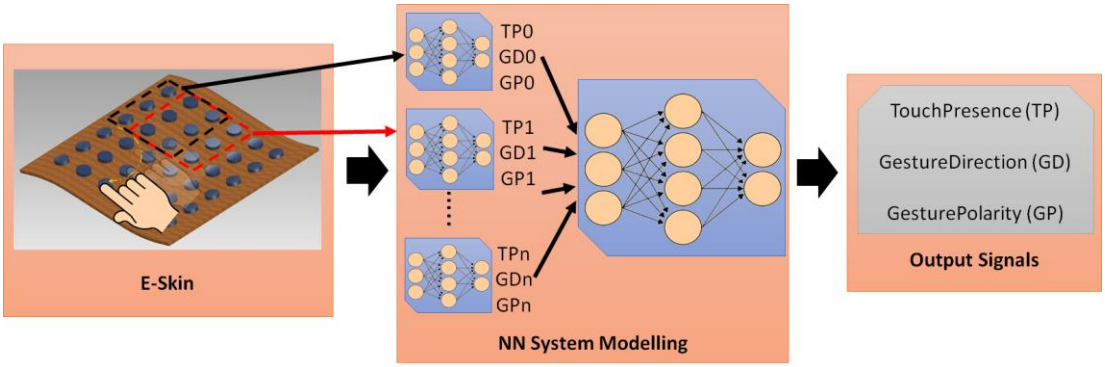
$$R_{TotReverse} = R_{Q-Pre-neuron} + R_{Q-Post-neuron} + R_{SM} \quad \textbf{(E8-4)}$$

To demonstrate the effectiveness of the proposed approach and to advance it to system level, a tactile information processing problem was simulated as explained in the next section.

8.1.2.1.3. System Modelling

The schema of the sparse coding system shown in Fig. 8-10(a) comprises of an array of tactile sensors (6x6) which acts as an input to the NN system model. The target of the current sparse coder is to encode the tactile input or gesture into three outputs 'TouchPresence', 'GestureDirection' and 'GesturePolarity'. The outputs are considered as bits depending on whether the neuron is on or off. 'TouchPresence' is a single bit output which signifies downstream reduction i.e. whenever one of the tactile sensor (out of the 6×6 sensors) is touched, the output should be on, as shown in the second column of Fig. 8-10(b). This could be used as an event driven triggering stage for triggering the higher stages of a neural network. 'GestureDirection' is a 4-bit data output for which the values 0001, 0010, 0100, 1000 correspond to the directions NE to SW, N to S, NW to SE and W to E respectively. The reverse direction for each case has the same output value for 'GestureDirection' except that 'GesturePolarity' is set to 1 instead of 0, as shown in Fig. 8-10(b). The model was implemented in two levels. The lower NN level (Simbrain snapshot shown in Fig. 8-10c) acquires input from a 3x3 sub-array of the e-skin to a 9 thresholded tactile receptor decay neurons. Since, the feeling of gestures on the skin depends on sensory memory, the above application serves as an effective way of testing the proposed approach. Hence, the sparse coder was modelled as a combination of a Decay Neuron Network forming an input layer followed by a feedforward neural network. The simulations were performed on SimBrain [309]. The decay time depends on the time of the sensory or short term memory decay in equation (3). (Supplementary section 3 of [33] shows the snapshot of the time series plot of decay of the simbrain simulation of four neurons with different decay constants). The decay

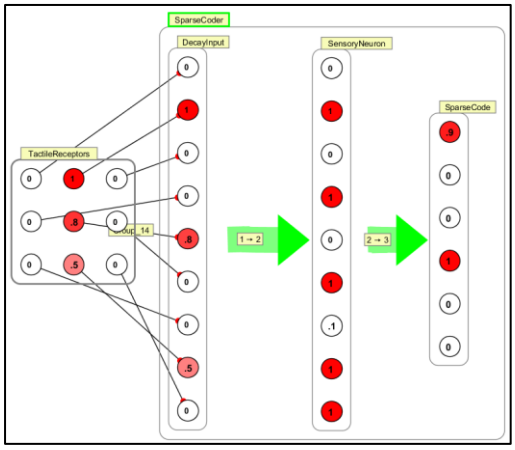
neuron forms the input to a sparse coder. From a system viewpoint, this 3x3 sparse coder could be considered as a low-level cell. In a hardware implementation, this could be realised with NWs-based lower level cellular structure in the backplane of 3x3 tactile sensors sub-array. This approach enables achieving hierarchical upstream reductions. The level 1 sparse coder was modeled and trained in Matlab using the Levenberg-Marquardt method with 9 logistic hidden layer neurons corresponding to 9 sensory neurons feed forwarded to 6 output neurons. The input and target for training, validation and testing the sparse coder as per Fig. 8-10(b) was generated using a Matlab code generating various tactile gestures based on a random number generator. A total of 5000 samples were generated out of which 3500 samples were used for training, 750 samples for validation and further 750 samples for testing the system. After training, the weight and bias matrices were transferred to SimBrain for testing and visualisation. Based on the simulation, training and validation, it was found that the dataset was linearly separable and was implementable with a single layer neural network with the output converged to a mean squared error of 0.02 for linear output neurons-implying a zero error as with the logistic or binary output stage. Fig. 8-10(c) shows the typical implementation on SimBrain where the output of the receptor is passed to the sensory neuron through the decay inputs. The sensory neuron and the higher level logistic neurons together perform the sparse coding of the input to outputs as in Fig. 8-10(b). The first 3 blocks in Fig. 8-10(c) together mimic the functionality of the sensory neuron of the circuit given in Fig. (a). Fig. 8-10(d) shows the mean squared error Vs epochs during training of the network. The network converged within 30 epochs, giving a mean squared error of 0.02. In the next section, the interface of a tactile skin to a higher level NN (level 2) through many such level 1 cells to emulate tactile gesture recognition is presented.



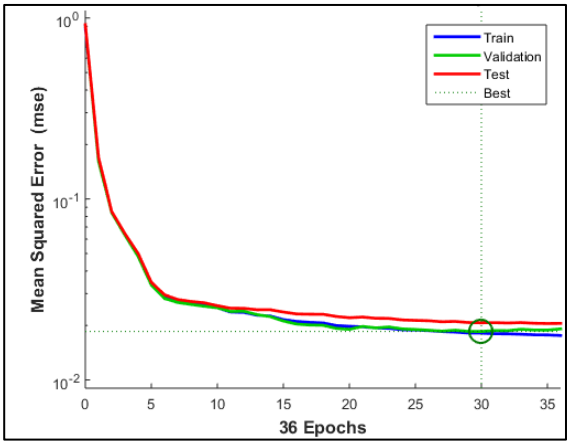
(a)

Typical Illustration									
Touch Presence	0	1	1	1	1	1	1	1	1
Gesture Direction	0000	0000	0001	0001	0010	0010	0100	1000	1000
Gesture Polarity	0	0	0	1	0	1	0	0	1

(b)



(c)



(d)

Fig. 8-10: (a) Schematic illustration of Sparse coding of tactile data from e-skin neural information. (b) Goal of the sparse coding. (c) Typical implementation of one Level 1 sub neural network cell on SimBrain; the output of the decay sensory neuron is passed to the input of the sparse coder which gives the sparse coded output. (d) Mean squared error vs. epochs during training of the network. [33]. Frontiers:CC by 4.0.

8.1.2.2. Experimental Results

8.1.2.2.1. Kirigami-inspired e-skin on Prosthetic Hand Interfaced to System Model

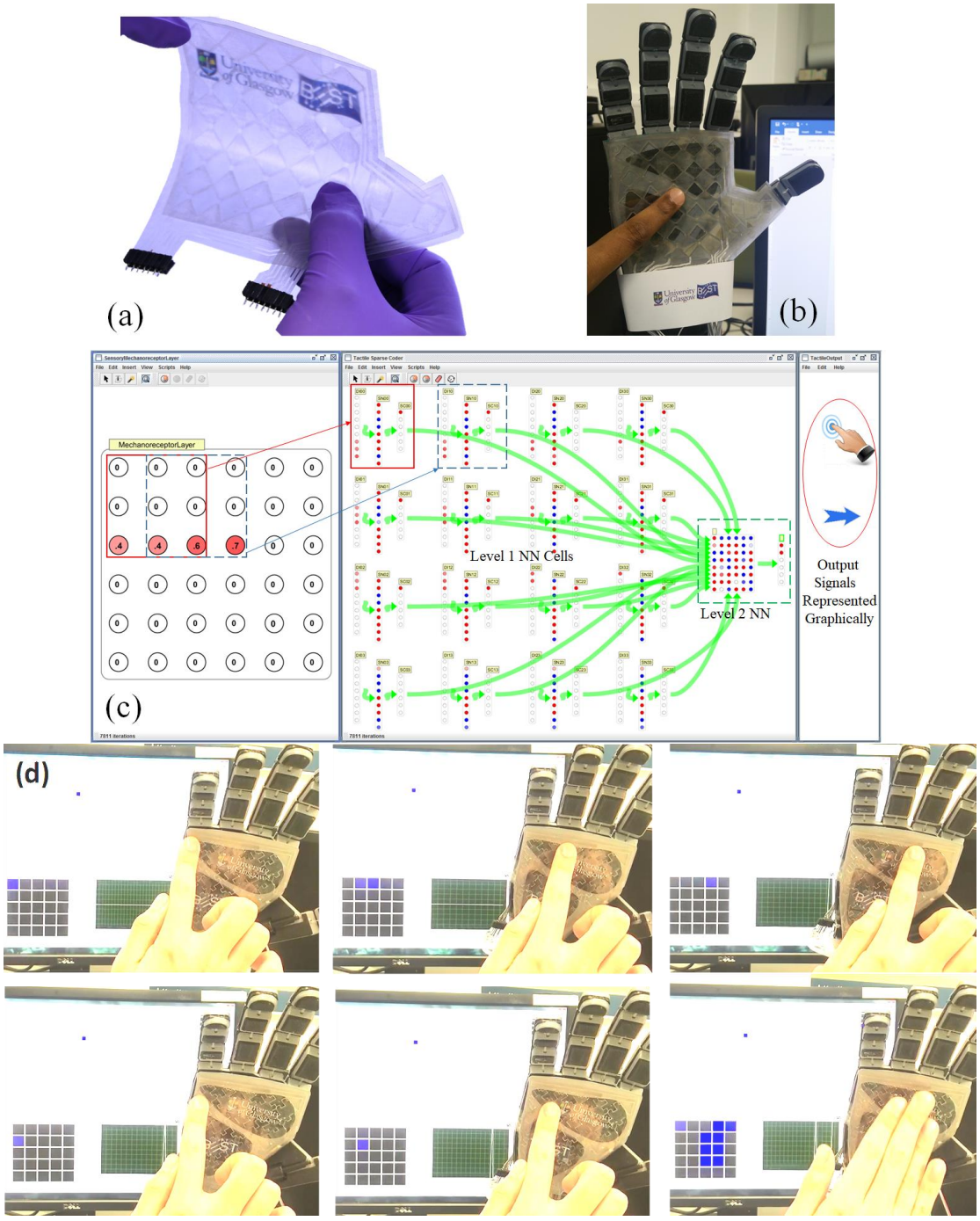


Fig. 8-11: System model interface with e-skin on prosthetic hand (a) Flexible and transparent touch sensitive e-skin (b) Image of the prosthetic/robotic hand with electronic skin (c) Snapshot of SimBrain model showing mechanoreceptors layer and associated sensory processing level 1 NN cells are connected to higher hierarchical level 2 NN block. Video of the demonstration in Supplementary section of [33]. (d) testing of tactile skin for single touch and multitouch input [33]. Frontiers:CC by 4.0.

The fabricated flexible and transparent touch sensitive e-skin is shown in Fig. 8-11(a). The fabricated passive tactile sensitive e-skin integrated on a 3D printed prosthetic/robotic

hand (Fig. 8-11(b)) was interfaced to the system model and tested in real time. The testing of the skin in the palm region for single and multi touch is shown in Fig. 8-11(d). Fig. 8-11 (c) shows the snapshot of SimBrain model showing mechanoreceptor layer comprising of 6x6 elements. The 3x3 overlapping window of receptor elements are connected to individual local processing level 1 NN cells as shown in Fig. 8-10(a) and Fig. 8-10 (c). The output of all level 1 NN cells correspond to an array of 96 elements form the input layer for another hierarchical level of the feed forward neural network comprising of 48 neurons in the hidden layer and 6 neurons in the output layer. The value of the output layer of NN shown in Fig. (c) indicates touch or direction events given in Fig. 8-10(b). The output signals corresponding to the value of the output layer are graphically represented in the third window of Fig. (c). The video of the demonstration is included in Supplementary section 4 of [33].

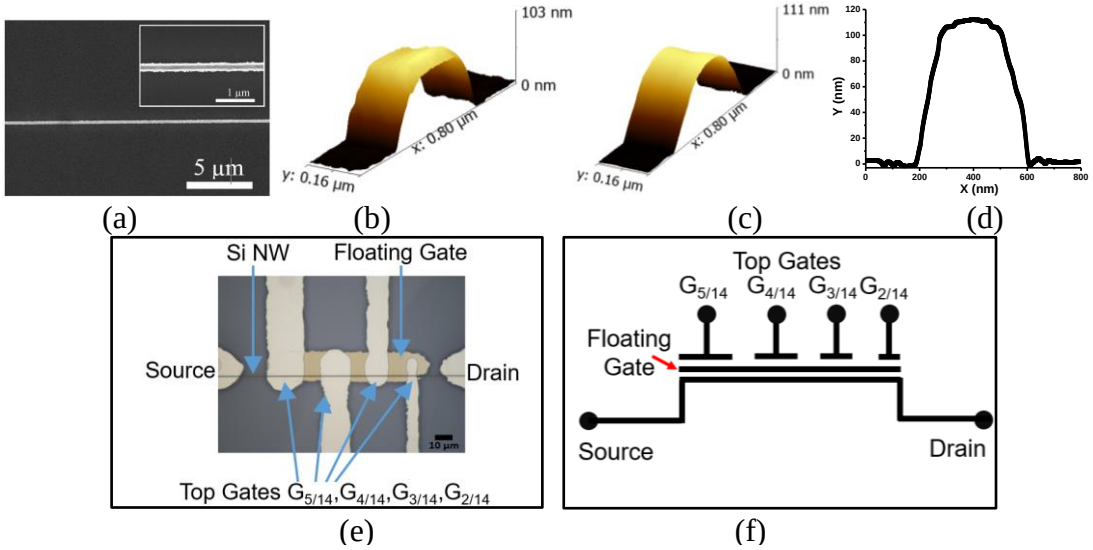
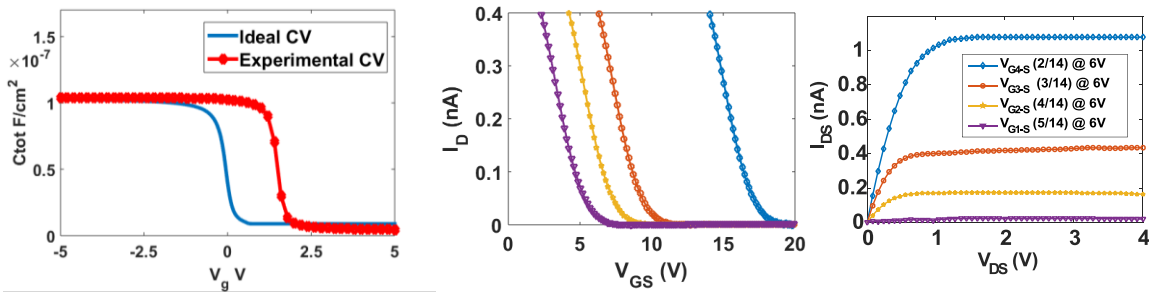


Fig. 8-12: (a) SEM image of NiCr nanoline in low magnification. This pattern is subsequently etched into trapezoidal NWs (Inset: High magnification). Three-dimensional AFM scan of SiNW taken (b) before atomic layer deposition (ALD) and (c) after ALD & thermal annealing processes; (d) Line profile corresponding to the AFM image (b) where a ~45º trapezoidal structure is observed. (e) Optical microscopy image of the fabricated υ-NWFET . (f) Symbolic representation and weights of the fabricated υ-NWFET. [33]. Frontiers:CC by 4.0.

8.1.2.2.2. Characterisation of υ-NWFET

The structural and electrical characteristics of Si υ-NWFET are presented in this section. As shown in the SEM images in Fig. 8-12(a), the fabrication process (described in Fig. 8-4(a-l)) results in a NiCr nanoline of width 200 nm which was used as a hard mask during dry etching for obtaining the Si NWs. After fabrication step shown in Fig. 8-4(f), the Si-NW was characterised by using AFM before and after Al_2O_3 deposition and doping (Fig. 8-12 (b)-(d)). The Si-NW has a thickness of ~100 nm after etching, as shown in the AFM image in Fig. 8-12(b). After ALD processing and doping, the surface is smoothened as depicted in Fig. 8-12 (c). The optical microscopy image of a fabricated prototypical υ-NWFET is shown in Fig. 8-12(e). In the fabricated four-gated υ-NWFET, the gates spanned 25 µm, 20 µm, 15 µm and 10 µm over the floating gate electrode, result in synaptic weights of around 5/14, 4/14, 3/14 and 2/14 respectively as illustrated in Fig. 8-12(f). Here, C_{FG} is not included as the capacitance between the floating gate and the NW is negligible compared to the

capacitances formed by the metal gates. Hereafter, the gates are referred, based on their synaptic weights, as $G_{5/14}$, $G_{4/14}$, $G_{3/14}$ and $G_{2/14}$.



(a) (b) (c)

Fig. 8-13: Electrical characteristics of Si υ-NWFET. (a) Ideal (blue) and experimental (red) C-V_g relationship. (b) V_{GS} vs. I_{DS} characteristics for $G_{5/14}$ to $G_{2/14}$ at V_{DS} = 4 V (c) V_{DS} vs. I_{DS} characteristics while applying 6 V to each gate, one by one. [33]. Frontiers:CC by 4.0.

The turn-off voltage of the υ-NWFET is influenced by the presence of various charges and interface trap density in the dielectric. The Pt/Ti-Al_2O_3 (80 nm)-Si stack was studied using Capacitance-Voltage (C-V) characterisation with a Keysight 1520A Capacitance Measure Unit. The Capacitance was measured for a gate voltage in the range of -5 to 5 V at 1 MHz frequency with a 50 mV-rms a-c signal. Both the ideal C-V and the experimental C-V curves are plotted in Fig. 8-13(a). Here, we used a Matlab code to obtain the ideal C-V curve by solving Poisson's equation [224]. The work function of the electrode (Ti), average doping concentration and the oxide thickness are defined as input parameters in this code. The value of flat band capacitance (C_{FB}) was obtained from the ideal C-V curve at V_g = 0V. This C_{FB} was used to get the flat band voltage (V_{FB}) the experimental C-V curve (V_{FB} = 1.6 V). The fixed oxide charge density was calculated (Q_{OX} = -1.43×10^{12} e-cm^{-2}) by finding the flat band voltage shift. The interface trap density D_{IT}, calculated using the Terman method, was found to be in a range of 1.39 - 7.89 x10^{12} $eV^{-1}cm^{-2}$. The ideal and practical threshold voltages (V_{th}) are ~0.6 V and ~2.2 V, respectively. In the case of a floating gate structure, the effective voltage needed on the floating gate (50nm from channel) is less than the inversion voltage observed from the C-V characteristics. Further, the additional charges in the floating gate dielectric interface will result in deviation from the ideal turn off voltage (expected ~1.4 V). Fig. 8-13(b) shows the V_{GS} Vs I_{DS} characteristics with voltage sweep applied to the gates of the υ-NWFET one at a time, while others kept at 0 V. Since the presented υ-NWFET works in depletion mode like a gated resistor, the channel depletes with an increase in the gate voltage, finally inverted, resulting in a decrease in the current. The dependence of the observed turn-off voltage (i.e. 6.1 V, 7.7 V, 9.8 V and 16.8 V (rounded to 1 decimal point for gates 1 to 4 respectively) on the synaptic weight of each gates demonstrates the working of the υ-NWFET. Fig. 8-13(c) shows the transfer characteristics of the υ-NWFET as each gate is given 6 V, one at a time. The gate with higher synaptic weight suppresses the current more compared to the gate with the lower synaptic weight in the order $G_{2/14}$ to $G_{5/14}$ with current reduced ~54 times from 1.0772±0.01 nA to 19.6±0.1 pA at V_{DS} = 4 V and V_{GS} = 6 V. The difference between the trend in the simulation presented in

Fig. 8-6a, b and actual data Fig. 8-13(b), c could be attributed to the fact that the υ-NWFET presented here works as a gated resistor in depletion mode in contrast to the simulation. The gates with non-equal width were given voltage one at a time while the rest were at zero potential in contrast to the simulated device. Further, from the current values,

the contacts appear to be Schottky-type, whereas simulation considers a perfect ohmic contact. The early saturation observed in this long channel υ-NWFET could also be attributed to the saturation in one of the Schottky mode contacts. Higher performance could be obtained in a sub-50 nm υ-NWFET with optimised contacts. The results herein clearly indicate the expected neuronal function from the υ-NWFET device.

8.1.2.2.3. Effect of Fabrication Induced Gate Weight Variability on the Performance of System Model

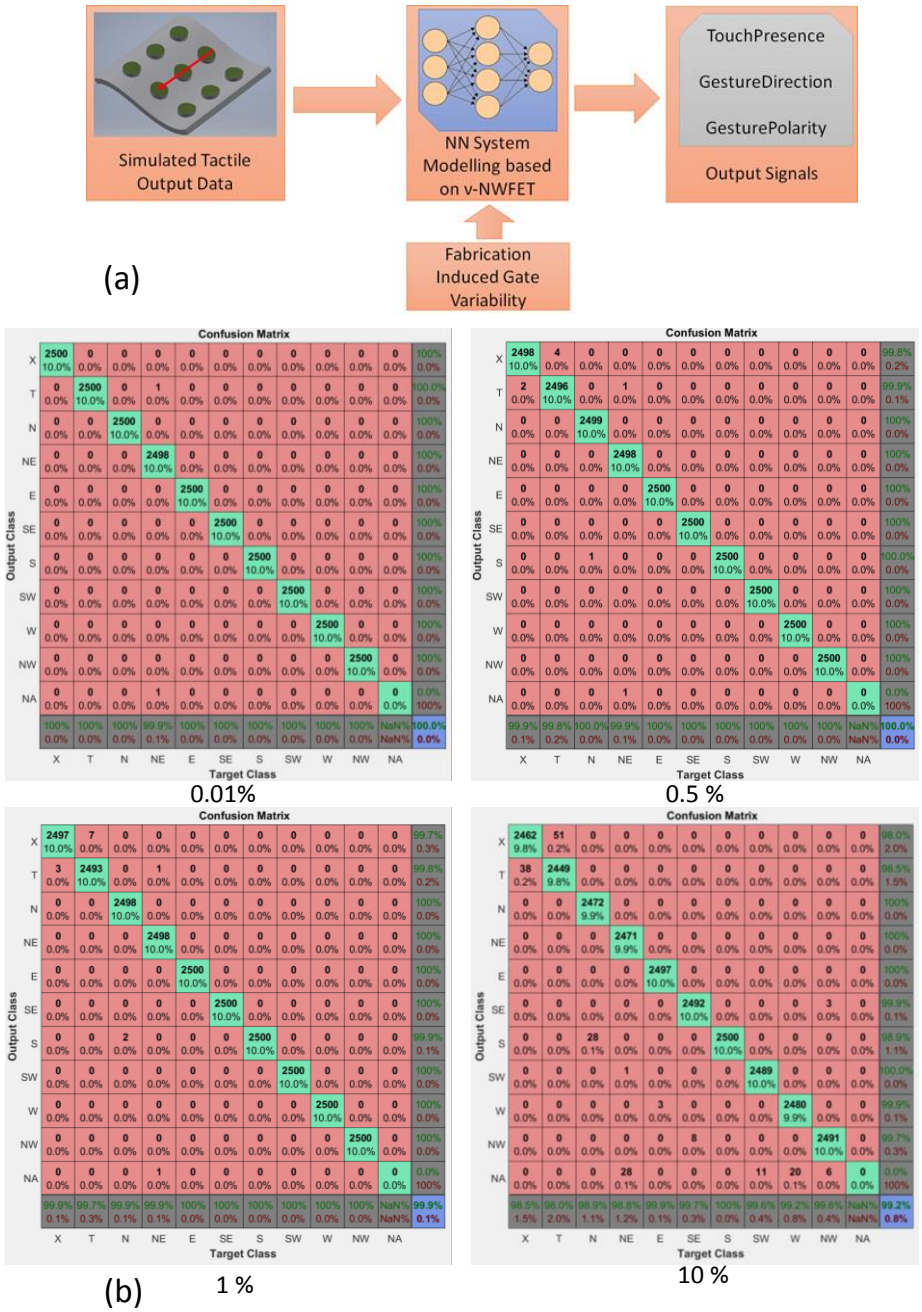


Fig. 8-14: (a) Schematic to study impact on neural function of the NN due to the deviation in weights (b)Effect of weight deviations on the NN's performance[33]. Frontiers:CC by 4.0.

The system model given in section 8.1.2.1.3 were used to understand the potential impact on neural function of the resulting network due to the deviation in gate weights arising from the line-edge roughness during fabrication (seen in Fig. 8-12e). This is schematically

illustrated in the Fig. a. The line-edge roughness results in variation in the capacitances compared to the design value. By fitting the cut-off voltage obtained in the previous section, the experimental capacitances were obtained. The results are compared with the design capacitances in Table 21. A deviation of ~ <0.1% are observed between design and experimental capacitances. The weights of the system model were changed using a random number generator to maximum of 10% to check its effect on the sparse coder. The results are plotted as confusion matrices in Fig. b. The class values in the x and y-axis namely, X, T, N, NE, E, SE, S, SW, W, NW, NA corresponds to No Touch, Touch, North, North East, East, South East, South, South West, West, North West and Not Applicable respectively. With 0.01% weight deviation, only 2 out of 25000 classifications were misclassified. For 0.5%, 1% and 10% deviations the number of samples that were misclassified were 9, 14 and 2546 samples out of 25000 were misclassified which shows the inherent robustness in NN.

Table 21: Comparison of designed capacitances with experimental capacitance for various gates.

Capacitance	$G_{5/14}$	$G_{4/14}$	$G_{3/14}$	$G_{2/14}$
Design	1.3812 pF	1.1050 pF	0.8287 pF	0.5525 pF
Experimental (Fit)	1.3932 pF	1.1037	0.8672 pF	0.5059 pF
Deviation (%)	0.00869	0.00118	0.04887	0.08434

8.1.3. Discussion

The υ-NWFETs based approach for realising HNN has several advantages for tactile data processing in electronic skin (e-skin). For example, it allows implementation of neural circuits in a compact array architecture [308]. With good subthreshold control of a tri-gated or gate all around NWFETs, [310] it would also be possible to develop highly power efficient devices or circuits. Further, the possibility of printing NWs [46,28,170] means with υ-NWFETs it will be possible to develop bendable or conformable systems, which is much needed for better integration of e-skin on curved surfaces such as the body of a robot or prosthetic hand [44]. Such e-skin could have printed υ-NWFETs in the backplane [20,46] to communicate with higher perceptual levels. It is possible to have 3D integration or stacking of NWs based circuit [92] and if such work is extended for e-skin then we may see more advantages, particularly, in terms of mimicking biological tissues and brain. The integration of υ-NWFET based neural processing circuits with NW-based neural recording/mapping and stimulation circuits is another direction that could significantly advance the research in neuro-prosthetics, bio-neuro interfaces and electroceuticals [221,311,303,312].

While the direction is interesting and promising, there are significant challenges associated before realising a fully biomimicking artificial tactile skin. The tactile data processing in biological e-skin is much complicated and has complex pathways. The notion of neurons being represented as entities performing weighted summation followed by actuation itself is a significant approximation far from a real neuron, and a slightly more closer approximation uses time-domain differential equations to explain biological neuron's membrane dynamics and interaction [313].

Biological neurons are highly energy efficient compared to most artificial implementation of neurons [314]. To achieve energy efficiency and better performance, a

υ-NWFET should have lower leakage current, higher drive current and higher on-to-off ratio. High-K dielectric used as a gate dielectric to avoid gate leakage while still having lower EOT ensures better coupling and control of gates over the channel. Further, the gates formed in a trigate configuration around the NW offers better subthreshold performance. On-to-off ratio of up to 2.6 x 10^4 was achieved for the simulated device structure with all gates ON Vs. all gates OFF. For packing more neurons per unit area and improving performance further, the υ-NWFET must be scaled in all dimensions such as the width, length of the NW, the gate span of each gates.

When such intense scaling is carried out, the process variations such as variations in doping concentration, NW dimension, gate width, line edge roughness may influence the synaptic weights and performance of the neural network. However, neural networks are known to be inherently fault tolerant and robust. In the presented work, comparison of designed capacitances with experimental capacitance shows a maximum fabrication induced weight variation ~0.1%. Allowing up to 1% change in the weights of the system model lead to misclassification of the data set by only ~0.06% which shows the robustness of NN for such applications.

The various circuit approaches presented could be used as sub-components for neuro-mimicking tactile e-skin and based on system requirement, choice can be made between hardwired-neuron with no plasticity (as in Fig. 8-7), neuron with plasticity having sensory memory or STM (as in Fig.) or LTM(as in Fig.) to be used at different hierarchical levels of the tactile sensing NN. Synaptic plasticity finds application both in data storage/memory as well as neural computation. In the first approach, i. e. hardwired-neurons, learning and circuit/layout synthesis will be through software tools which will be followed by practical fabrication forming a hardwired neural network. By introducing additional plastic synapse schemes (as in Fig. or Fig.), the weight could be modulated over the initial value set by the capacitances. In this case the synaptic weight initially set by the capacitances could be considered as a phyletic memory [315] because it is hardwired over which further schemes of plasticity operates. Such an approach could be considered as a semi-plastic neural network. For such a network, the quantisation arising from layout synthesis (For example rounding-off the weight equivalent capacitance dimensions to 1 μm) followed by lithography process for fabricating the capacitors will lead to k-levels of possible discrete synaptic weights [316,317]. The approach proposed in Fig. results in a programmable synapse, which could be used to implement hardware-in-the-loop learning. It is to be noted that in the initial stage of tactile sensing the sensory data need to be stored only for a short time and hence a neural circuit with sensory memory is sufficient for earlier tactile data handling as in Fig. . This circuit could be further modified for higher hierarchical levels to have STM and LTM associated plasticity. A transitionary circuit from sensory memory to STM can be achieved either by replacing the C_{SM} with an element of higher value (as in Fig. (c)) or by replacing $Q_{forward}$ with a nanoionic-like transistor [305] for use in higher hierarchical level of neural network beyond tactile skin. Beyond that, increasing C_{SM} may not be a practical option as it becomes bulkier in the process of realising longer times. Possible strategies for transition from STM to LTM at different stages of the network include replacing $Q_{forward}$ by a nanoionic-like transistor [305], or with a NW-based programmable floating gate transistor [93], or replacing $R_{forward}$ with a memristive device [297].

The system model interfaced with a flexible and transparent touch sensitive e-skin with 6x6 tactile elements and tested in real-time demonstrates the working of the proposed

approach. However, since the SimBrain model involves software NN programmed in java to mimic the HNN, a delay of ~1.12-1.54s was observed per cycle for the implementation with Intel® Core™ i7-4500U CPU @ 2.4 GHz with 8GB RAM and a delay per cycle of ~0.394-0.470s was observed for implementation in Intel® Core™ i7-4790K CPU @ 4 GHz with 32GB RAM. While this could be improved by approaches such as use of GPU, dedicated HNN such as the proposed approach will be optimal for real-time tactile data processing. The delay with software NN will be much substantial if the number of tactile elements are increased for example to a human palm ~18675 MRs as shown in Fig. 2-12. Further advancements in the system model is required towards advanced tactile perception tasks such as schematically shown in Fig. (d).

One of the potential application of this technology could be in an industrial task such as fruit or object sorting, where the bio-mimicking neural networks in the skin of robotic hands could classify and held objects based on the physical parameters such as pressure, temperature etc. as well as optical parameters from special optical sensors from tactile e-skin [184,44].

8. 2. Summary

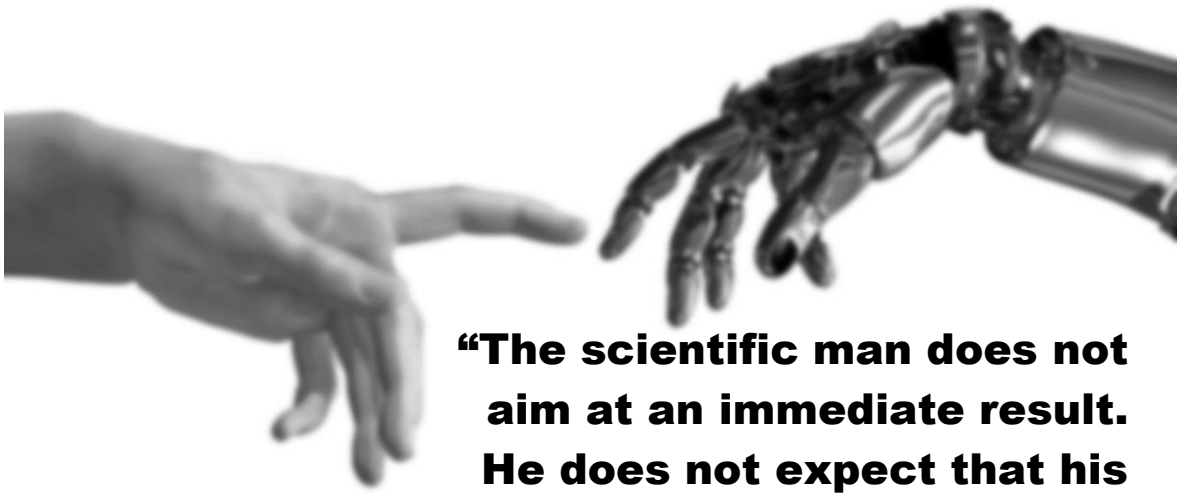
A υ-NWFET based approach for realising hardware neural networks has been presented and validated through device, circuit and system-level modelling and simulation. Two different approaches, STM and LTM, have been simulated to implement the memory or neuroplasticity. Fabrication of a υ-NWFET has been carried out with a Si-NW as the channel material. The I-V characteristics of the υ-NWFET demonstrates the neuronal function of the device with synaptic weights modulating the output current. For example, for a given drain (V_{DS} = 4 V) and gate voltage (V_{GS} = 6 V), the drain current at output was reduced by ~54 times with a gate weight of 5/14 as compared to 2/14. The proposed structure is a step towards realising flexible power-efficient bio-inspired neural sensing and circuit architectures as a backplane for tactile e-skin in robotics or prosthetics.

To this end, the system model interfaced with a flexible and transparent touch sensitive kirigami-inspired e-skin (having 6x6 tactile elements in the palm) and tested in real-time demonstrates the working of the proposed approach. The e-skin was fabricated on ITO by expanding the capacitive sensing structures discussed in chapter 4 section 4. 2.

Up to 1% change in the weights of the system model lead to misclassification of the data set by <0.06% which shows the robustness of NN for tactile sensing application. In principle, the approach could be adapted for spiking neural networks and further exploration in that direction should be extremely interesting. Multilayer or deep learning hardware neural networks could be used for further additional sparse coding to enable advanced tactile perception tasks such as schematically shown in Fig. 8-1(d) but requires scalable fabrication. Future work will include large area fabrication of the proposed e-skin system in a flexible form factor and its subsequent testing.

9

Conclusions and Future Work



“The scientific man does not aim at an immediate result. He does not expect that his ideas will be readily taken up. His work is like that of a planter — for the future. His duty is to lay the foundation of those who are to come and point the way”
-Nikola Tesla, 1900

Contents

9. Conclusions and Future Work

Investigation of IMNS-based technologies for flexible electronics and specifically, electronic skin application has been presented in this thesis. Multiple forms of IMNSs are explored namely: ultra-thin chips, micro/nanowires, ribbons, and polycrystalline film on foil. Sensors and active components were realised based on these structures. The works done as a part of this doctoral thesis and future directions are illustrated in Fig. 9-1.

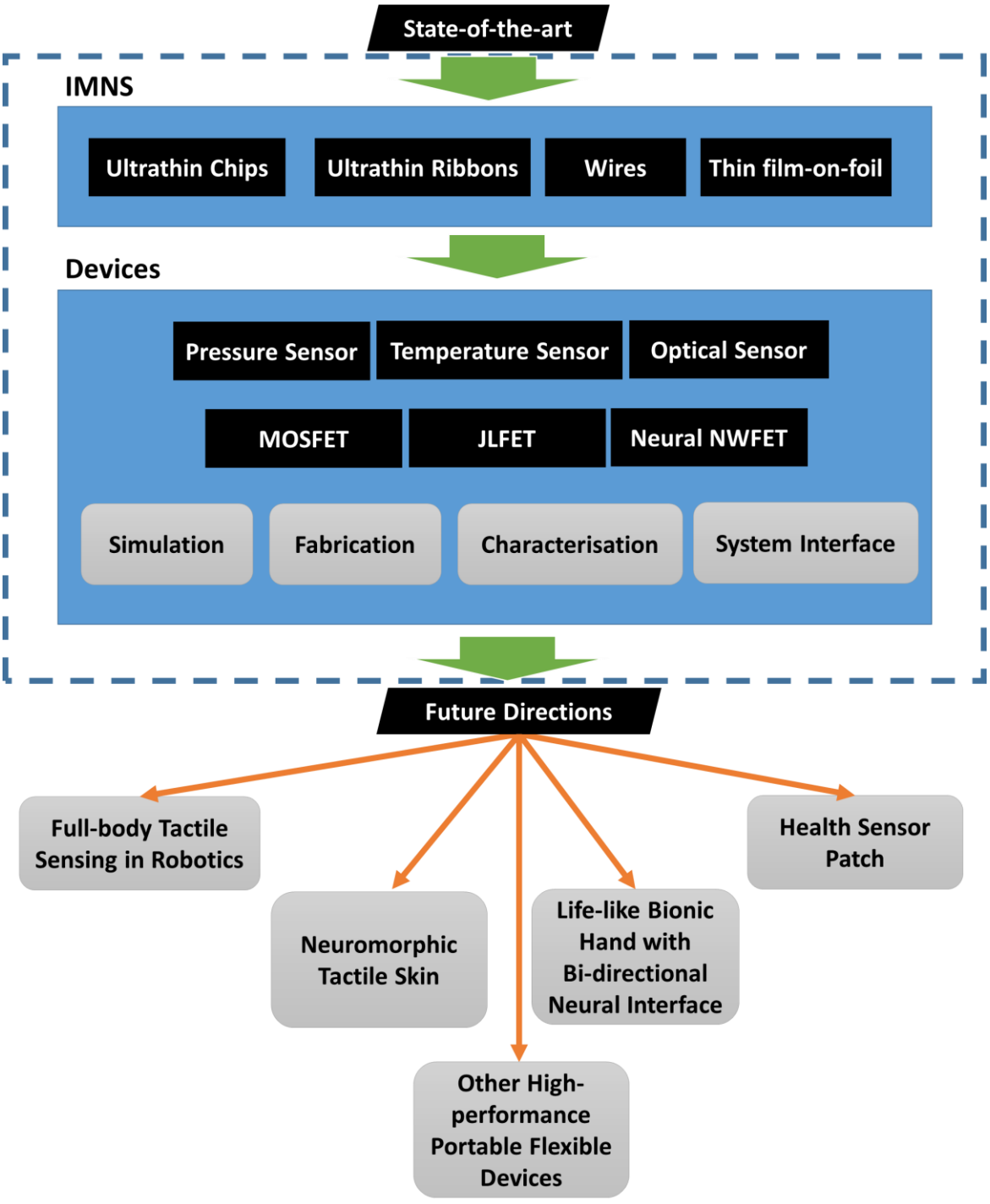


Fig. 9-1: Illustration of research work carried out and future directions

9. 1. Conclusions

Sensors:

A capacitive-piezoelectric tandem architecture sensor for biomimetic tactile sensing has been conceptualised and fabricated from indium tin oxide (ITO) thin film on poly ethylene terephthalate (PET) sheet. The results are presented in chapter 4. The sensor exhibited both dynamic and static sensory capability. The non-linearity of the static capacitive structure with higher sensitivity (0.25 kPa^{-1}) at low pressure range (<100 Pa) is desirable mimicking how mechanoreceptors behave in human skin. The piezoelectric sensor on the base of the stack, still exhibited a linear response with sensitivity of 2.28 kPa^{-1}. The sensors are attractive for prosthetic and robotic tactile sensing.

V_2O_5 nanowires were aligned between electrodes to realize a non-contact temperature sensor. The details and results are presented in chapter 7. The sensitivity was found to be 55.5 Ω/K or 0.03% /K. The sensor is suitable for tactile e-skin application.

ZnO and Silicon nanowires were contact printed between flexible electrodes to realize a Wheatstone bridge UV sensor for application in health sensory e-skin. The characterisation of the resulting UV photodetectors exhibited an excellent response to UV illumination with (I_{photo}/I_{dark} above 10^4) and a relatively better stability to thermal effects—thanks to the WB self-compensation mechanism.

Ultra-thin Silicon Wafer/Chip:

The first active component for high-performance flexible electronics based on IMNS presented in this thesis is MOSFET in flexible UTC form factor. Fabrication and wafer scale transfer of UTC with devices such as silicon MOS capacitors and MOSFETs were carried out. The various processes and results are presented in chapter 5. The chapter presents an innovative approach for wafer scale transfer of ultra-thin silicon chips on flexible substrates. The methodology has been demonstrated with various devices (ultra-thin chip resistive samples, MOS capacitors and n-channel MOSFETs) on wafers up to 4" diameter. This is supported by extensive electro-mechanical characterisation and theoretical analysis, including finite element simulation, to evaluate the effect of bending and the critical breaking radius of curvature. The ultra-thin chips on polyimide did not break until the radius of curvature of 1.437 mm. In the case of MOS capacitors the measured capacitance increases with an increase in bending load. The changes in the transfer and output characteristics of ultra-thin MOSFETs closely match with the theoretical values utilising empirically determined parameters. For a typical device, the estimated effective surface mobility for tensile, planar and compressive bending conditions were 384, 350 and 333 $cm^2/V\text{-}s$, respectively. The drain conductances at tensile, planar and compressive conditions were estimated to be 4.94, 4.58 and 4.06 μS/μm respectively. The on-to-off current ratios for the three cases were 4.32, 4.38 and 4.39 decades. The subthreshold slope for tensile, planar and compressive conditions were 1.06, 0.98 and 1.04 V/decade. The calculated gate delays were 0.23, 0.27 and 0.3 ns for tensile, planar and compressive conditions which implies ~3 GHz operation with a variation of ~11 to 15%.

Overall, the work demonstrates the efficacy of the new methodology presented here for wafer scale transfer of ultra-thin chips on flexible substrates. The presented research will be useful for obtaining high-performance and compact circuits needed in many futuristic flexible electronics applications such as implantable electronics and flexible displays.

Further, it will open new avenues for realising multi-layered multi-material (foil-to-foil) integrated bendable electronics.

The MOSFETs were used in an extended gate configuration with the capacitive-piezoelectric tandem architecture tactile sensor modules.

Ultra-thin Silicon Membrane/Ribbon:

The second form factor investigated for high-performance flexible electronics is ultra-thin silicon ribbon structures. This is suitable for large-area electronics (macro-electronics). I conceptualised and simulated ultra-thin silicon ribbon based junctionless FETs (JLFET) for use in high-performance flexible printable electronics. This addresses the challenges associated with selective source/drain doping and realising printable CMOS circuits with inorganic nanostructures. By tuning the work function of the metal gate, normally-off operation can be achieved. TCAD simulation was carried out with Silvaco TCAD. The simulation suggests that with Pt as a gate and an appropriate doping, an on-to-off ratio of 10^7 is achievable for the n-channel JLFET with a current of 84 µA/µm. This leads to a current of 3.36 mA for a 40 µm channel width which is suitable for driving µLEDs for flexible display applications as well as niche futuristic applications such as optogenetics as presented in the future works. Towards device fabrication, optimised transfer printing of ultra-thin silicon ribbons was initially carried out and the results are presented in chapter 6. One iteration of fabrication of ultra-thin silicon ribbon based JLFETs was carried out. The result shows field effect with current in nA range for three nano-ribbons (40 nm thickness and 5 µm width). However, the doping, contact and sintering process has to be further optimised for realising a high-performance device. This is currently a work in progress.

Nanowires:

Chapter 7 presented the work carried out on the investigation of nanowires for flexible electronics. A temperature-assisted dip-coating system was conceptualised and developed for large-area self-assembly of silica microspheres/nanospheres. The assembled spheres were used to achieve metal mesh patterns with a hole diameter ranging from tens of nm to a few µm. The nano-mesh patterns were used to synthesize silicon nanowires by metal assisted chemical etching (MACE). A modified NSL and e-beam dots-on-the-fly lithography were also used for synthesising nanowires. Nanowires of diameter as low as 10 nm and of aspect ratio more than 200:1 were achieved. The synthesised silicon nanowires were heterogeneously integrated with bottom-up fabricated ZnO nanowires using contact printing to realize ultra-violet (UV) dosimeter structures as explained in the sensor section above.

Chapter 7 also presented the work done on the development of large-area DEP-assisted templated transfer printing of nanowires. V_2O_5 nanowires were assembled between electrodes to realize temperature sensors of sensitivity given above.

Apart from FET structures, a υ-NWFET based approach for realising hardware neural networks has been presented and validated through device, circuit and system-level modelling and simulation in Chapter 8 of the thesis. Fabrication of a υ-NWFET has been carried out with a top down fabricated Si-NW as the channel material. The I-V characteristics of the υ-NWFET demonstrates the neuronal function of the device with synaptic weights modulating the output current. For example, for a given drain (V_{DS} = 4 V) and gate voltage (V_{GS} = 6 V), the drain current at output was reduced by ~54 times with a gate weight of 5/14 as compared to 2/14. The proposed structure is a step towards realising flexible power-

efficient bio-inspired neural sensing and circuit architectures as a backplane for tactile e-skin in robotics or prosthetics.

Prosthesis Interface:

A 3D printed bionic hand has been designed and fabricated as a test platform for the e-skin. A kirigami-inspired electronic skin was fabricated from the ITO/PET sheet and interfaced with the developed prosthetic hand. To this end, the system model of υ-NWFET was interfaced with the flexible and transparent touch sensitive e-skin (with 6x6 tactile elements in the palm area). Real-time testing demonstrates the working of the proposed approach. Up to 1% change in the weights of the system model lead to misclassification of the data set by <0.06% which shows the robustness of NN for tactile sensing applications.

Salient features of this thesis include:

1) A novel capacitance-piezoelectric tandem architecture with floating electrode for biomimetic tactile sensing is investigated for the first time. The structure leads to a nonlinear sensitivity similar to human tactile sensing with very high sensitivity (up to 0.25 kPa-1) in the lower pressure range (<100 Pa) and lower sensitivity in higher pressure (0.002 kPa-1 at ~2.5 kPa). This tandem structure helps for both quasi-static and dynamic tactile exploration. For example, both static and dynamic feedback can be provided to the prosthesis users as explained in the use case[239,37]. Further, for tactile exploration application, the static sensor serves to maintain a stable pressure while the dynamic sensor can provide the details of texture variation which are suitable for accurately distinguishing or classifying tactile samples.
2) Wafer-scale transfer of UTCs realized from bulk silicon is the second key achievement of this thesis which advances the state-of-the-art with scalability and cost-effective fabrication.
3) Investigation of junctionless FETs for flexible electronics has been carried out for the first time which can lead to scalable large-area high performance flexible electronics.
4) The developed contact printing setup and non-contact large-area DEP process during this research could find application for heterogeneous and scalable integration of various nanomaterials for futuristic smart systems.
5) The viability of Si nanowires (NWs) as the active material for υ-NWFETs to realize hardware neural networks is a key contribution. By using the above printing strategies to print NWs on large area flexible substrates, it will be possible to develop a bendable tactile skin with distributed neural elements (for local data processing, as in biological skin) in the backplane.
6) The work has demonstrated how prosthesis and robotics can be advanced using large-area high-performance flexible electronics and what features a next generation prosthesis will have. The demonstrated technologies include: biomimetic tactile sensing, a kirigami-inspired patterning strategy to conformally cover the prosthesis, myoelectric control with the capability to offer static and dynamic force feedback, a flexible solar-cell array and supercapacitors for energy harvesting.

9. 2. Future Work

Table 22: Biomedical Applications of Flexible Electronics [318-321,1,322,50]

Surgical Procedures • Video endoscopes • Smart catheters • Swallowable smart pill	Implants • Sub-retinal implants • Smart pace makers • Electrical Recording of Heart signals • Other systems for blind vision	Actuators • ICD defibrillator • Electroceuticals • Optogenetics
Flexible Electrodes • Electrocardiography (ECG) • Electromyography (EMG) • Electroencephalography (EEG) • Electrocorticography or intra-cranial EEG (iEEG) • Intracellular recording using electrodes • Nanowire FETs based cellular recording	Sensors • pH and other bioanalyte sensors • Blast sensor patch in sports/military helmets to detect trauma injury • Ultra-violet (UV) sensor patch to sense the UV dose exposure throughout the day • Pulse oximetry sensor patch • Fruit freshness sensor • Sensing H_2S gas from fruits • Flexible MRI Coils • Ocular pressure sensors • Smart contact lens • Wireless implantable pressure sensor • Insole Sensors	Neural Interface and Prosthetics • Tactile functional prosthetics • Neuro-prosthetics • Brain machine interface for exciting and sensing neurons • Neuro-morphic implantable biomedical system

To summarize, substantial work has been carried out to realize the various IMNS-based sensing and active components required to achieve e-skin with row column addressing and neuromimicking data processing (illustrated in Fig. 9-1). A fully biomimetic tactile sensing system is far from achieved, with mainly proof of concepts given in this thesis. Some attempts to integrate the different components to a system level interface on prosthesis has also been carried out as detailed in chapter 8 with further scope for advancements in several aspects. The immediate future work is

- to integrate the sensors (tactile, temperature) and active components (JLFETs, ν-NWFET) in a seamless way to realize large-scale and high- density electronic skin approaching or on par with the skin of the human hand. Sensors and backplane electronics has to be realized.
- The scaling up of the IMNS printing system to more than 10 times the size realised during this research (3 centimetres achieved so far). This will be the key to achieve the above.

- robust designs in different hierarchical levels and local neuro-mimicking classifiers along with scaling up of the IMNS printing system.

The approaches presented here will also help in realising a full body robotic skin for life-like humanoid robots as well as other biomorphic robots. The vital requirements to achieve full body humanoid robotic skin on par with human skin (Fig. 2-12) are robust designs in different hierarchical levels and local neuro-mimicking classifiers along with scaling up of the IMNS printing system. Practical realisation of the JLFET concept proposed in this thesis will be a step forward towards it.

This research also finds many futuristic applications mainly in the biomedical field. For example, the convergence of flexible electronics and biology has immense potential for many exciting future applications some of which are given in Table 22 and categorised as tools for surgical procedures, implants, actuators, electrodes, sensors and neural interfaces. Fig. 9-2 shows a typical application where IMNSs as electronic skin elements find application in various components of closed loop bidirectional neural prosthesis. It comprises of:

1) IMNS based e-skin with row/column readout and biomimetic data processing
2) E-skin for bidirectional neural interface with the capability of
   (a) reading the neural signals and interpreting them reliably to decode the prosthesis user's intention.
   (b) writing to the neurons to give feedback to the user.

Nanowire FETs find application in reading from the neurons [221,222], thanks to the higher sensitivity offered by the surface-to-volume ratio, as well as for decoding the neural signals such as spike sorting. UTCs can also be used for this application. There is already progress in this direction as presented in a conference publication[323], where flexible ultra-thin chips for neural interface was realised based on the technology developed during this doctoral thesis. Currently, there is no stable, long lasting, reliable solution for writing to the neurons. Conventionally, direct neural stimulation through longitudinal intrafascicular electrodes and more recently transverse intrafascicular multichannel electrodes, have been used to interface with peripheral nerves for sensory feedback [23,183,324,325]. Current direct neural stimulation has disadvantages in terms of causing structural changes within the nerve and the foreign body response to the electrode may induce encapsulation by scar tissue. This is observed in a recent human study with thin-film longitudinal intrafascicular electrodes where the sensory detection completely ceased after 10 days of electrical stimulation [326]. A promising solution is an optogenetic neural interface which uses genetically modified microbial opsins, or light-sensitive ion channels that are specific to nerves, for control of neural signalling [23]. The nerves can be excited or inhibited by specific wavelengths of light. Signal control at the biochemical level can be achieved with the optogenetics interface without physical contact between the nerve and the electrode. Towards optogenetic neural interface, ultra-thin silicon ribbon based JLFETs or UTCs presented on this thesis could be used as µLED drivers schematically illustrated in Fig. 9-2.

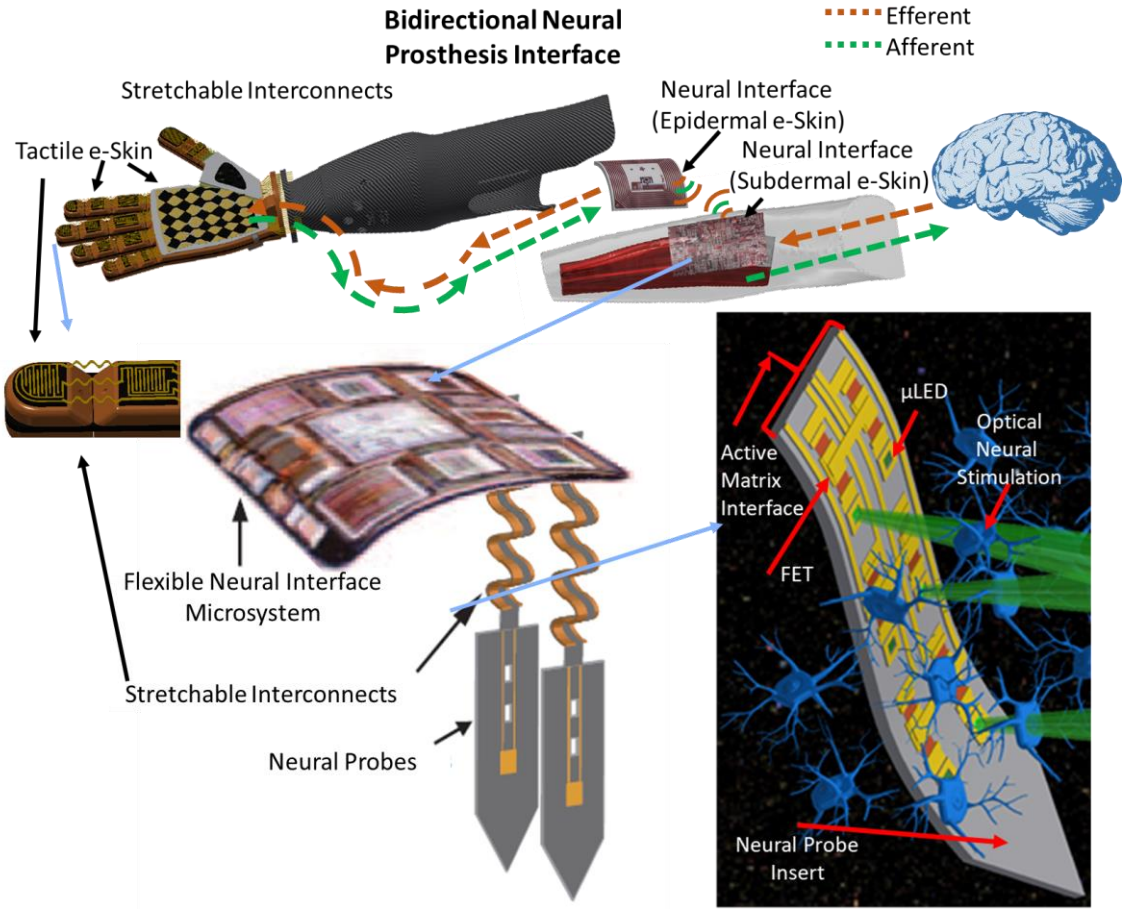


Fig. 9-2: IMNS as electronic skin elements for various components of closed loop bidirectional neural prosthesis.

Optogenetic neural stimulation currently seems to be an interesting pathway to achieve this [23] where signal control at the biochemical level can be achieved with the optogenetics interface without physical contact between the nerve and the electrode. Optogenetics requires compact light sources that can deliver light with excellent spatial, temporal, and spectral resolution to deep brain structures [6]. Optogenetics pulses of light with spatiotemporal precision are needed to stimulate the neurons. Typically, optogenetic stimulation is carried out by an external light source with fiber-optics to deliver the light to the targeted location. Typical driving requirements in such application are precise temporal requirement i.e. rise time and fall time (10% to 90% and vice-versa) of current pulses <100 µs and in some specific applications <1 µs with current level up to 1.5 A. Such an arrangement is cumbersome and involves tether.

Tether-free implantable miniaturised optogenetic systems are preferred in such cases and IMNSs based drivers could provide the required temporal and spatial resolution. Further, with IMNSs it will be possible to achieve multi-wavelength and multi-array microLEDs (µLED) targeting various optogenetic channels (corresponding to various opsins) such as channelrhodopsin[327], halorhodopsin[328], archaerhodopsin[329], and bacteriorhodopsin[26]. Towards an optogenetic neural interface, IMNS compound semiconductor structures and FET technology could lead to high density active arrays or matrix probes where IMNS based FETs are proposed to be used as µLED drivers.

Also, UTCs finds application as a gateway or interfacing chip between the neural interface (subdermal) electronic skin and external wireless transceiver (epidermal) electronic skin (Fig. 9-2) as well as for controlling the prosthesis in an efficient way. The high-performance of the UTCs serve to drive RF circuits and act as wireless powering circuits for the interface between the epidermal neural interface e-skin and the subdermal neural interface e-skin. A recent work carried out in collaboration with University of Toronto based on the UTC technology discussed in this thesis is a step towards such exciting directions[323].

Other applications include wearable e-skin with multi-sensors for health monitoring such as in a recently published work along with colleagues[50]. IMNSs find applications both as sensor elements as well as active high-performance components for RF drive electronics for such sensory skin.

Other applications include a smart tactile communication system for deaf-blind people [330]. Such smart assistive systems will not only enable bidirectional communication between people to people (disabled as well as normal) [330] but between people to futuristic assistive robots [331].

While there are interesting futuristic applications, it is to be noted that there are major challenges and hurdles for IMNS based technologies which have to be addressed and overcome. These include packaging, modelling, and dealing with thermal and stress-strain effects. A major reason behind the success of CMOS technology has been the availability of accurate models to predict the device response. This led to abstract models for use in CAD tools. However, this is challenging in the case of IMNS based flexible electronics as stress and various device architecture related effects must be considered in the model. Another important challenge where more and more research innovations and breakthroughs are required is in the scalability of the fabrication process. In conclusion, despite many challenges, the IMNS-based technology holds great promise for advances in many areas where high-performance flexible and conformable electronics are needed.

10. References

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